

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory / PEG/Display	3,4
CPU-Control/MISC/CFG/Audio/Power/GND	5,6,7
DDR4 Slot-DIMMA/B	8,9,10,11
PCH-LPC/SPI/SMBUS/MISC	12
PCH-Audio/Display/Clock	13
PCH-USB/PCIE/DMI/SATA	14
PCH-GPIO/RSVD	15
PCH-Power/GND/Strap	16,17,18
PCIE Slot-X16/X1/X4	19,20,21
ASM1083/PCI Slot	22,23
M.2 Card SLOT	24,25
M.2/SATA/PCIE SW	26
SATA Connector	27
USB POWER/PS2/USB2.0/USB3.0	28,29,30,31,32
ASM2142/USB TYPE A+C	33,34
LAN Intel I219	35
ITE6516-VGA/DVI/HDMI Connector	36,37,38
AUDIO ALC887	39
SIO-NTC6795D	40,41,42
CPU FAN/SYS FAN	43,44,45
ATX Power/F_Panel/ACPI-UPi Power	46,47
OV-NCT3933/GPIO-NCT5605	48
UP9508 VCore+VGT	49,50,51
CPU Power-VCCIO/VCCSTPLL/VCCSA	52,53,54
DDR4 Power-VCC_DDR/VPP25/VTT_DDR	55,56
PCH Core Power	57
SPI ROM/Clear CMOS	58,59
LED/Manual parts	60,61

MS-7B49

ATX
Ver: 1.1

Intel -Coffeelake plamform Z370

CPU: Coffeelake-S **System Chipset:** Z370

Onboard Chip:

HD Audio Codec : ALC887
LAN : Intel I219
SIO : Nuvoton 6795
Flash ROM : 16MB GSE Z370

Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI: NIKO/UPI **PWM:** UP9508

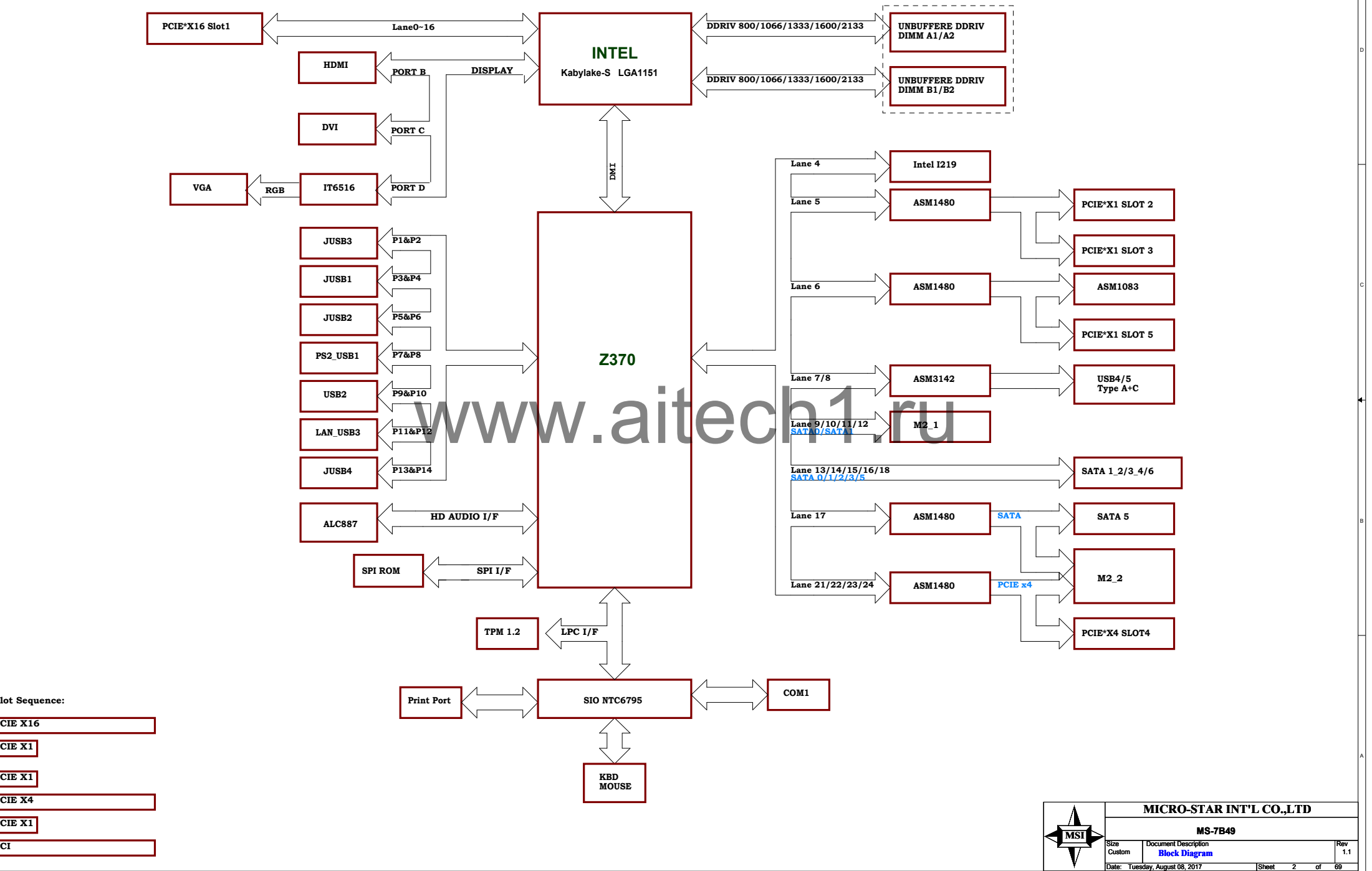
Expansion Slots:

PCI Express (X16) Slot *1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 3
PCI Slot * 1
M2 * 2 (22110 and 2280)

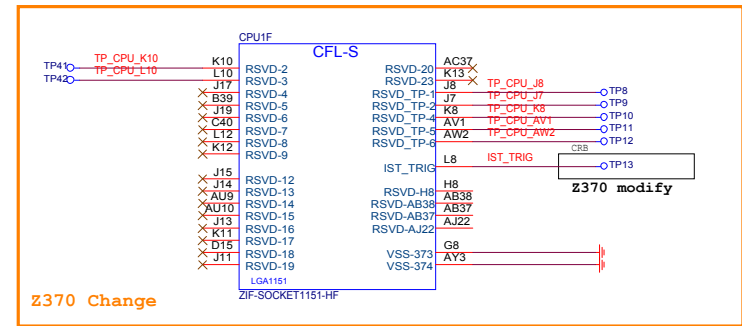
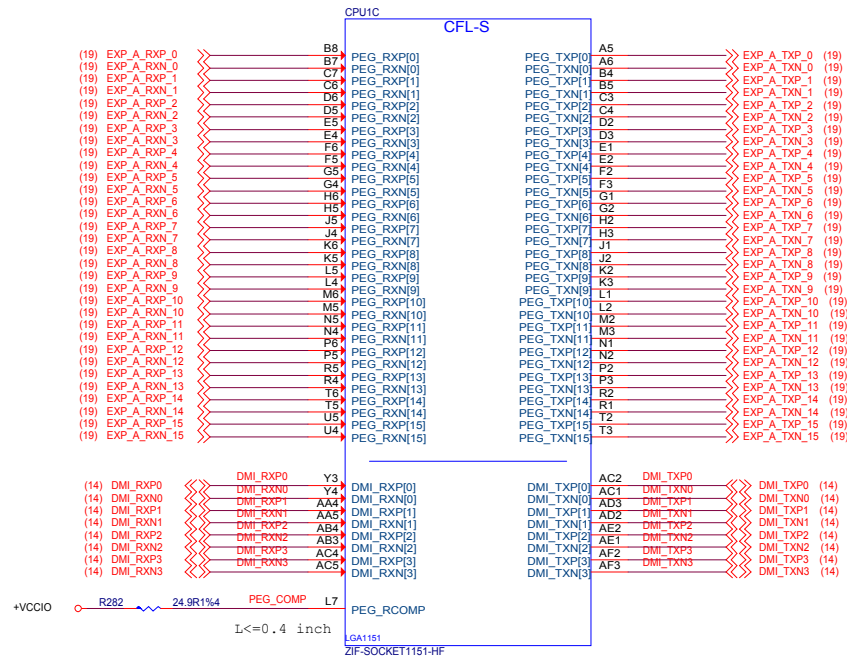
Other:

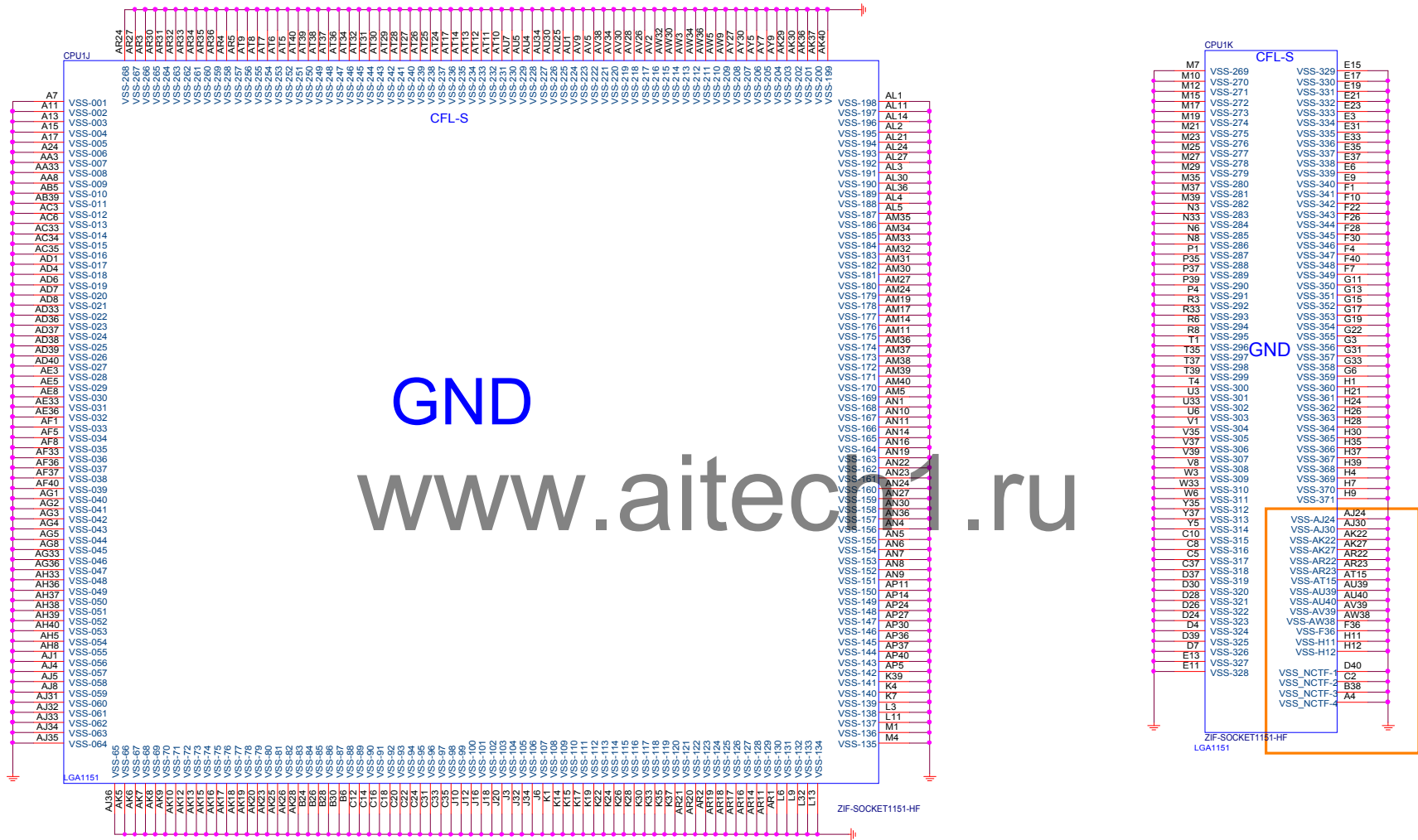
SATA3.0 x6 (PCH)
FRONT USB2.0 *4
FRONT USB3.0 *4
REAR USB2.0 *2
REAR USB3.0 *4
REAR USB3.1 TYPE A+C

MS-7B49 Block Diagram



- Slot Sequence:
- PCIE X16
 - PCIE X1
 - PCIE X1
 - PCIE X4
 - PCIE X1
 - PCI

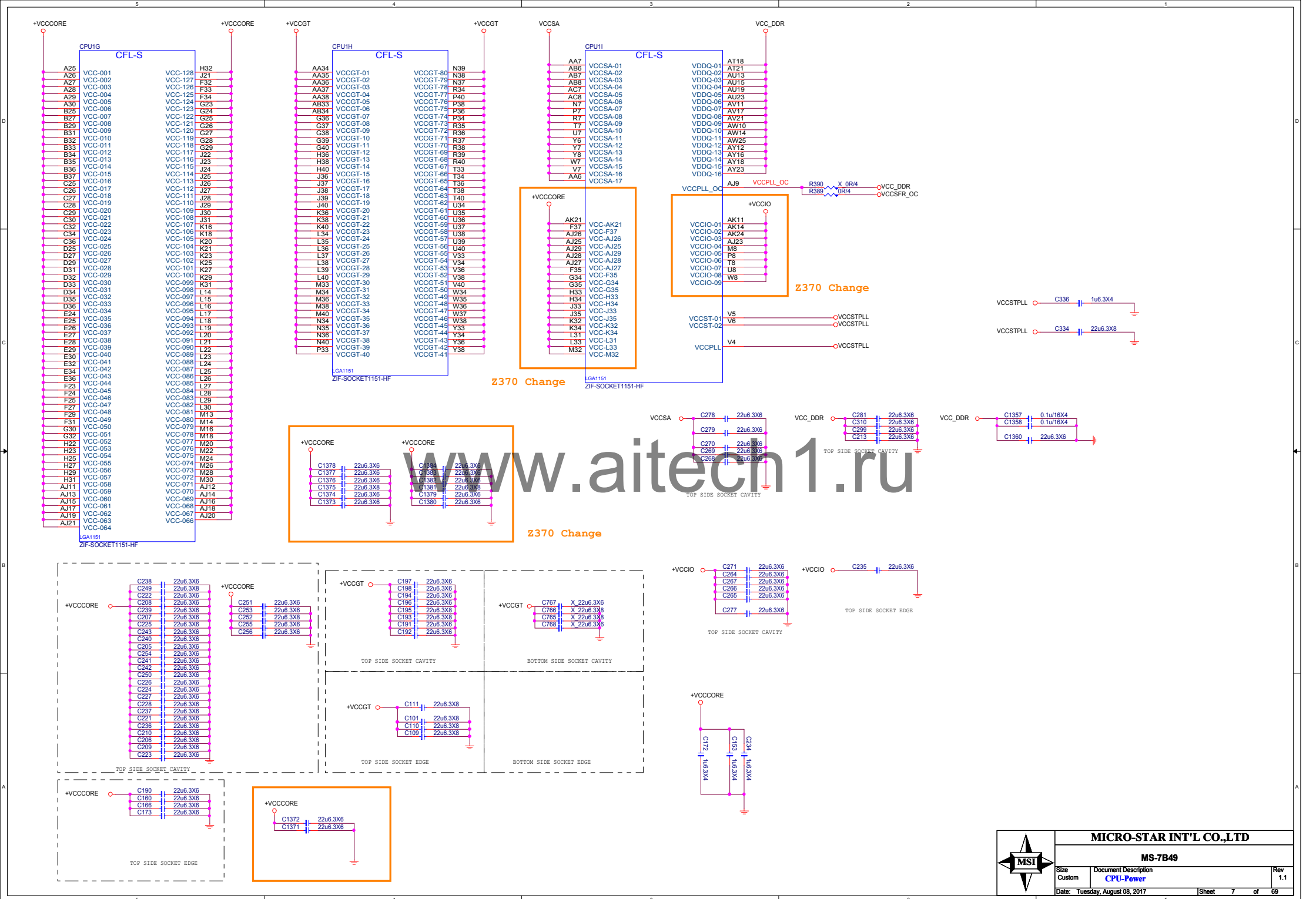


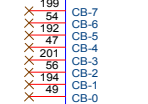
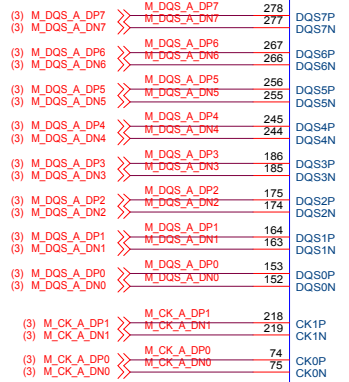
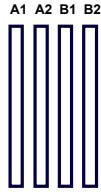


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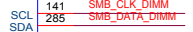
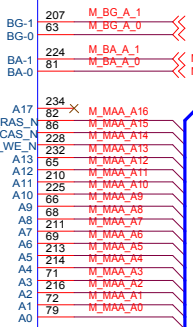
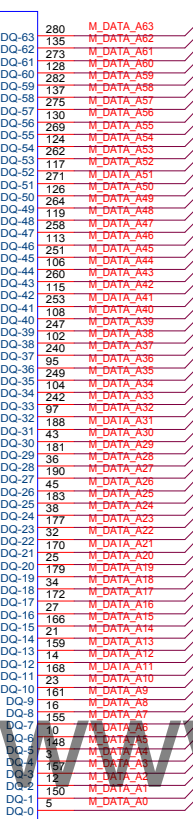
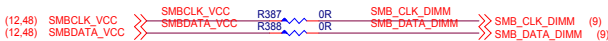
MS-7B49

Size	Document Description	Rev
Custom	CPU-GND	1.1
Date: Tuesday, August 08, 2017	Sheet 6 of 69	

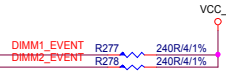




DDRIV-288P_BLACK-RH-21

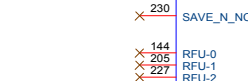
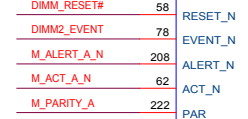
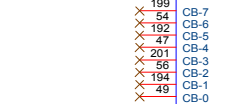
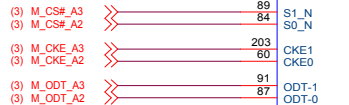
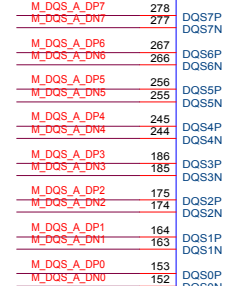


DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]



M_DATA_A[63:0] (3)

M_MAA_A[16:0] >> M_MAA_A[16:0] (3)



DDRIV-288P_BLACK-RH-21

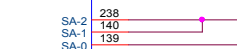
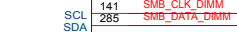
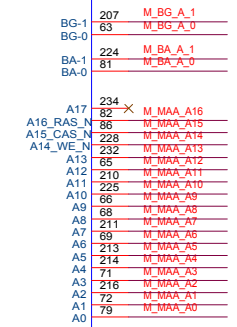
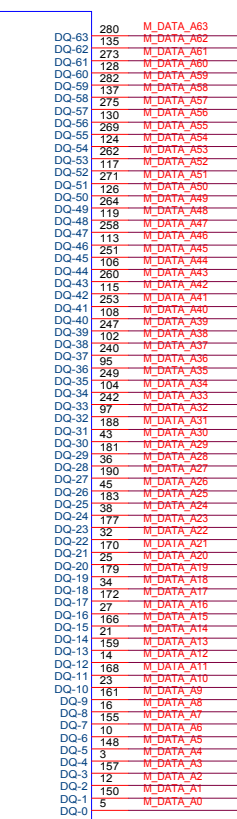


M_DATA_A[63:0] (3)

VCC_DDR



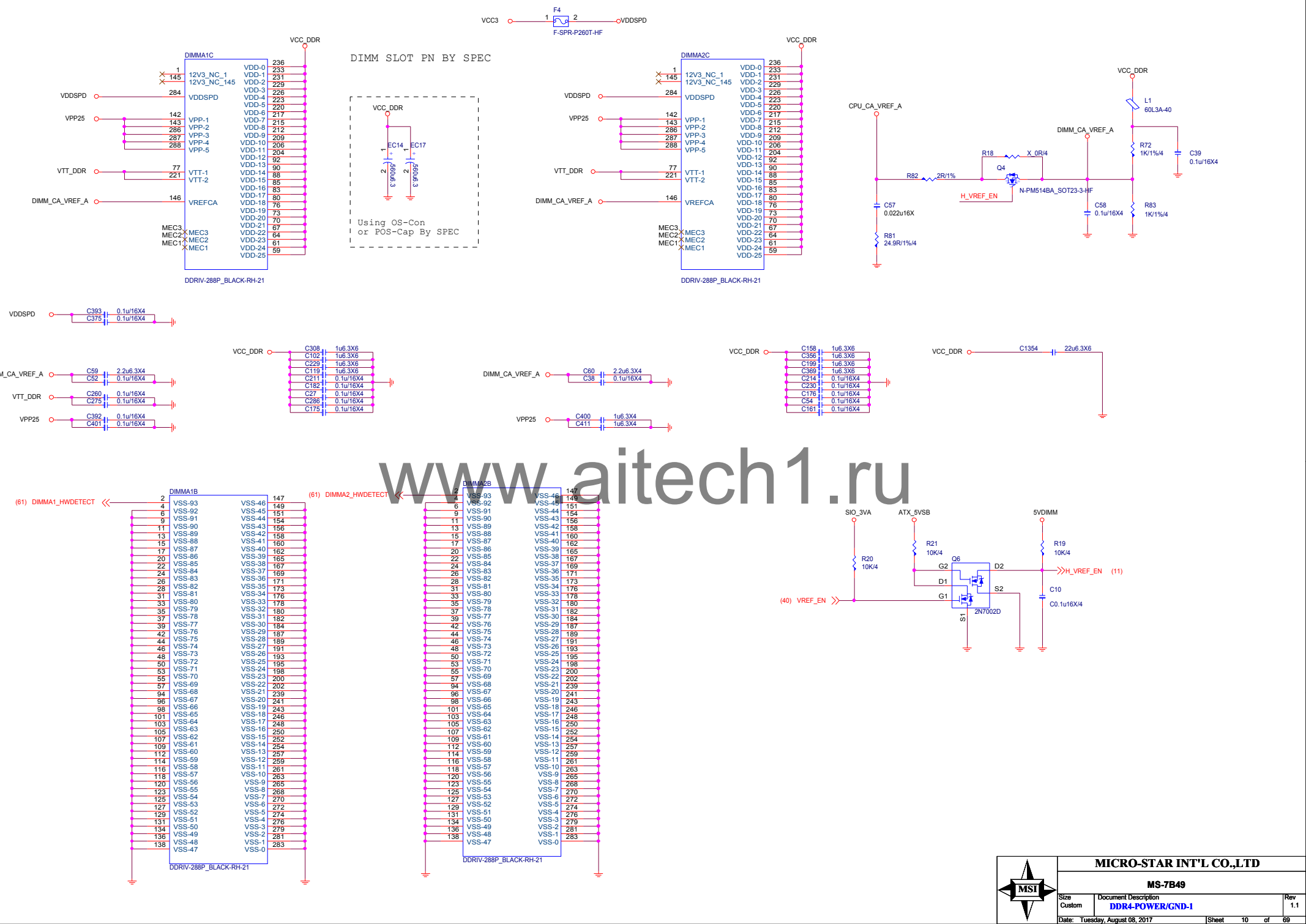
M_DATA_A[63:0] (3)

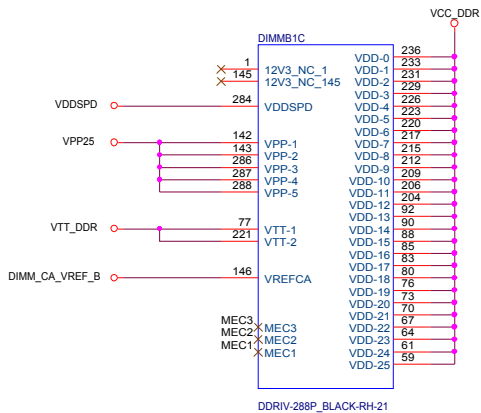


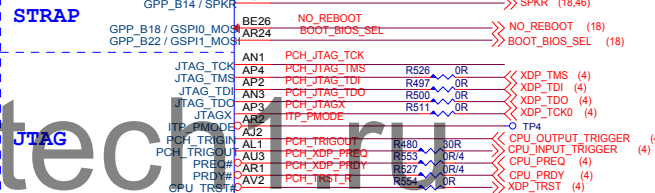
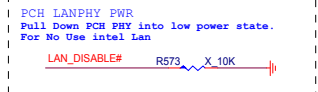
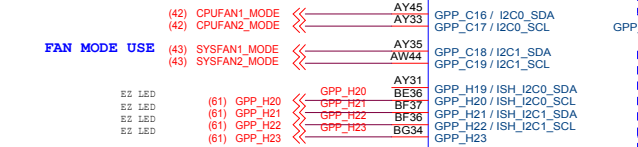
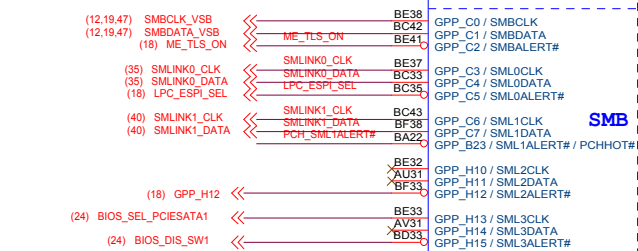
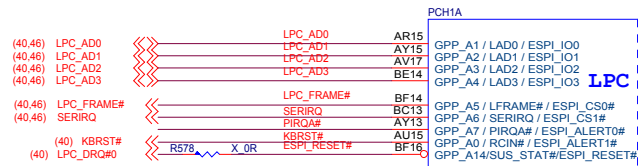
DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]



MICRO-STAR INT'L CO.,LTD		
MS-7B49		
Size	Document Description	Rev
Custom	DDR4 SLOT-DIMM1/DIMM2	1.1
Date: Tuesday, August 08, 2017		
Sheet 8 of 69		



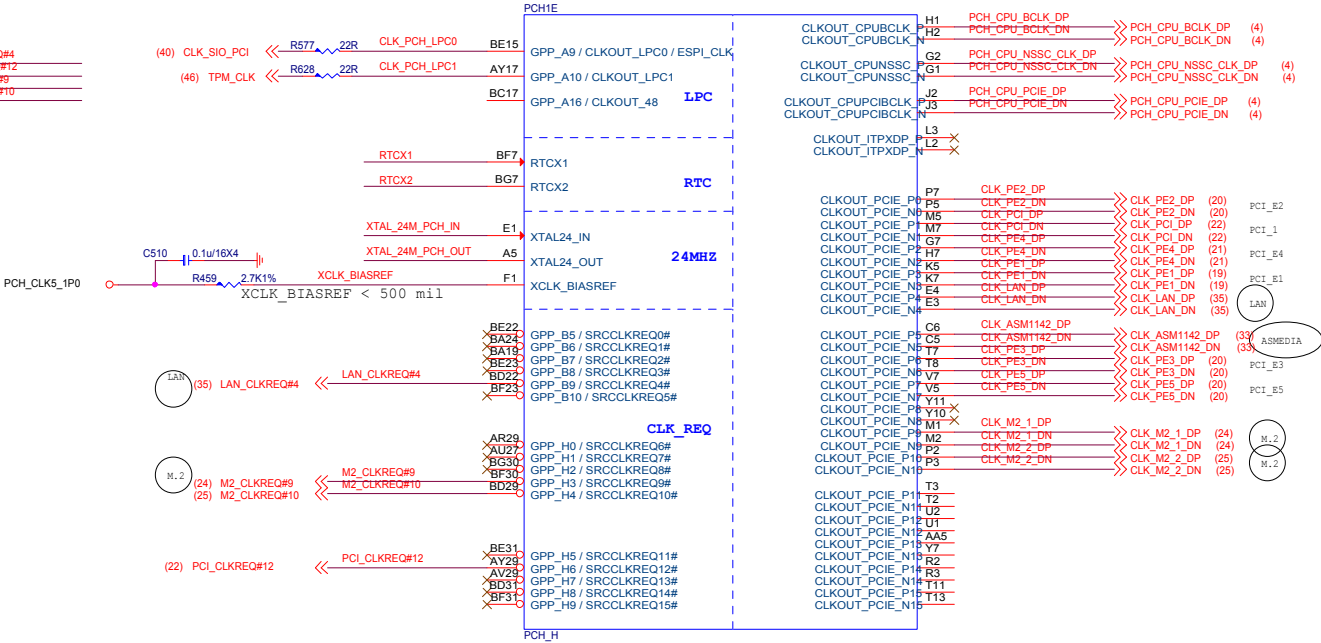
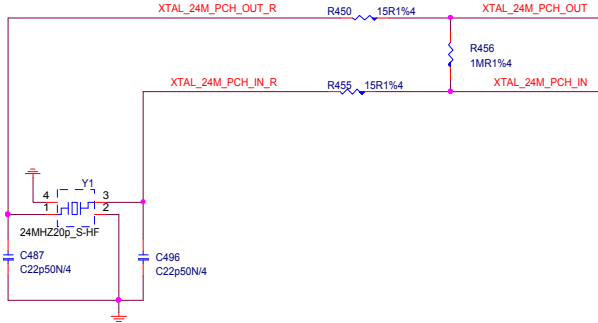
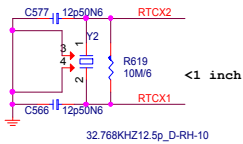




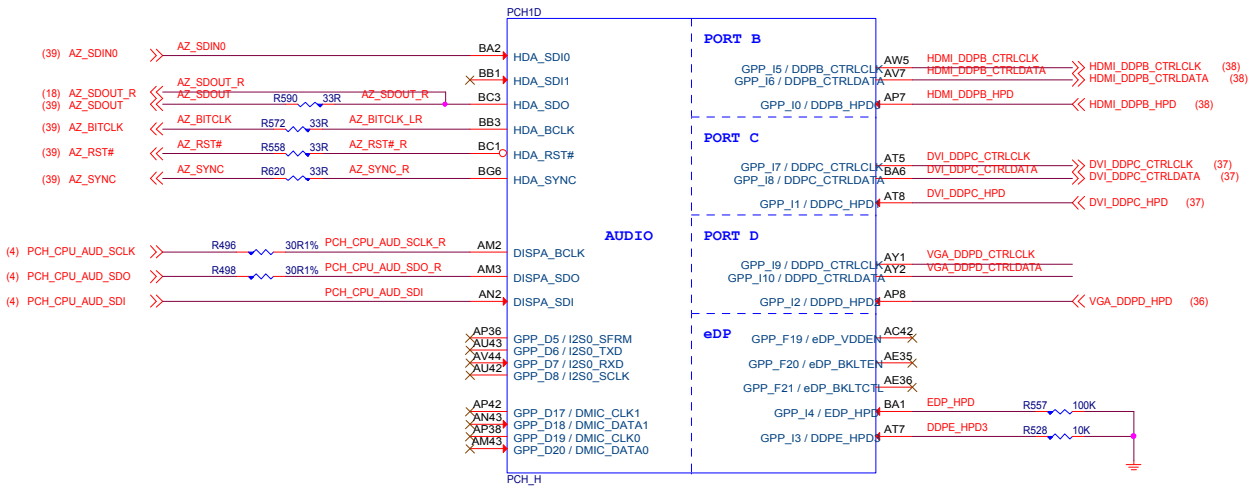
PCH_CLK


RTC Block

Close to PCH

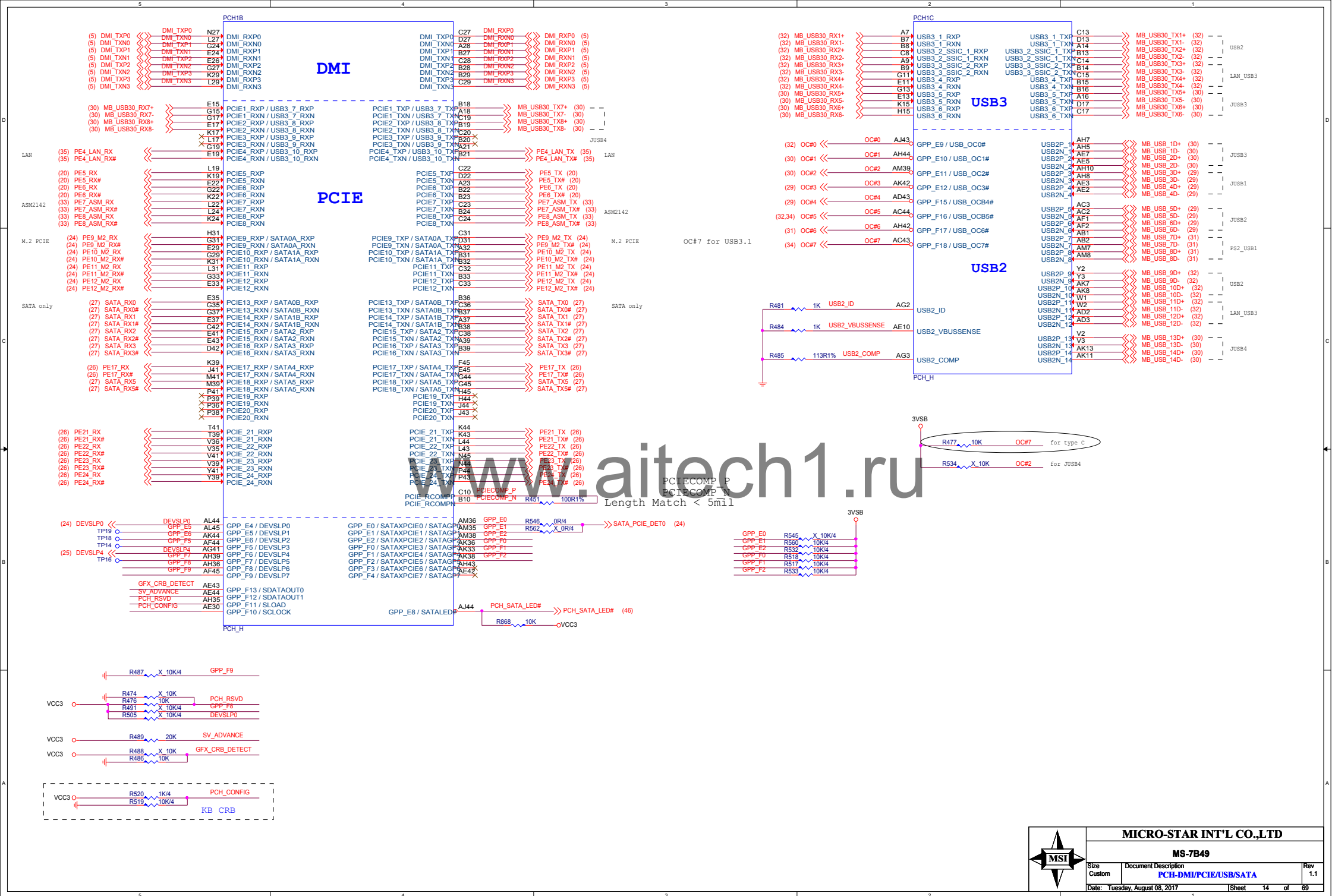


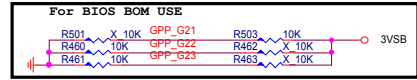
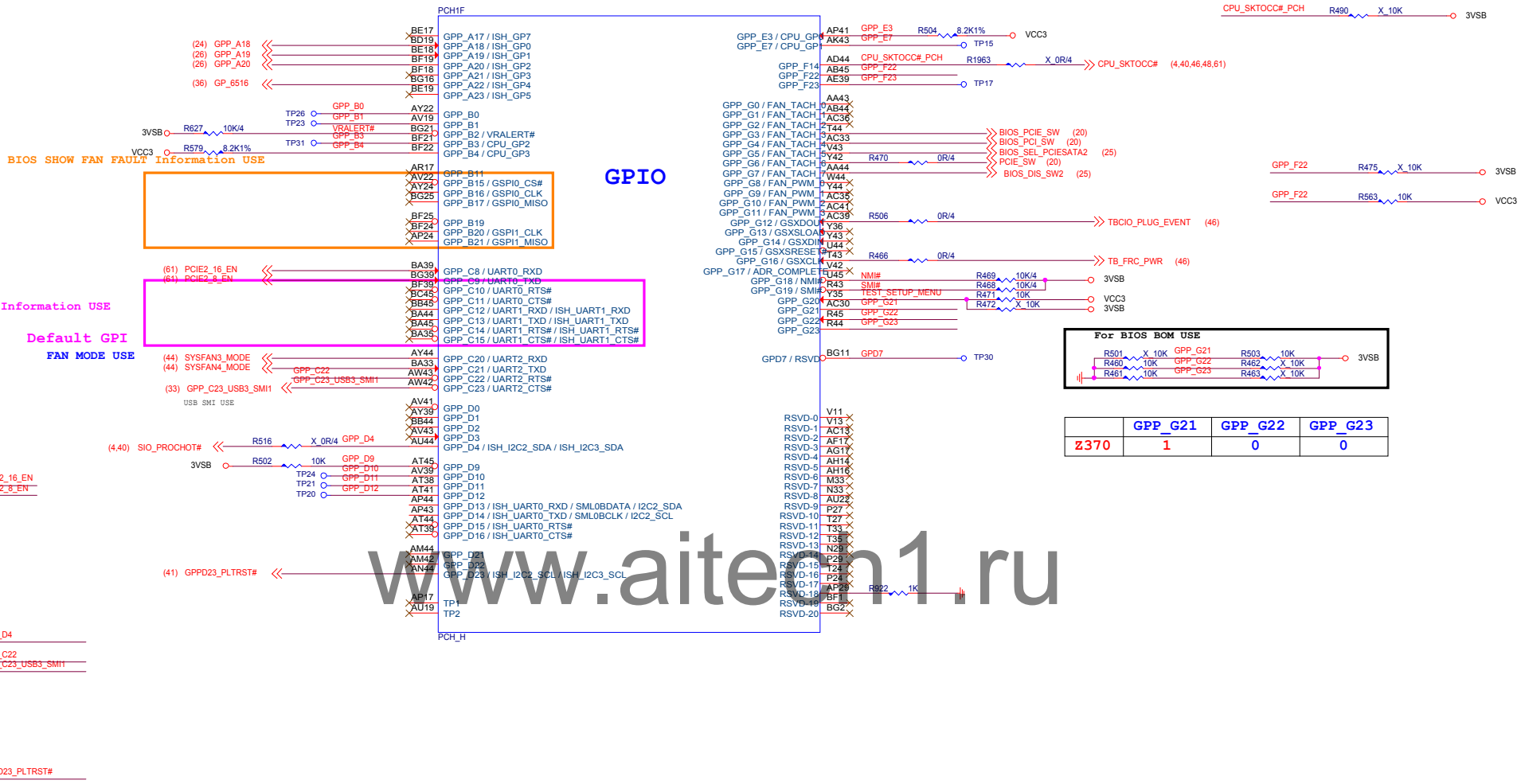
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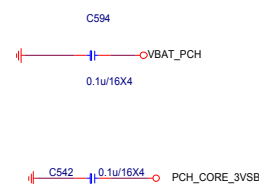
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MS-7B49		
Size	Document Description	Rev
Custom	PCH-Clock/Audio	1.1
Date: Tuesday, August 08, 2017		Sheet 13 of 69



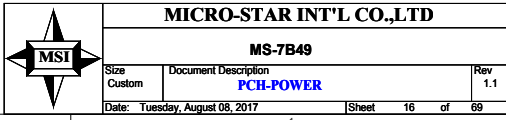


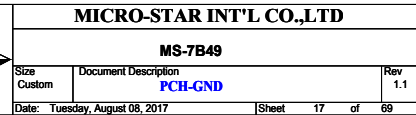
	GPP_G21	GPP_G22	GPP_G23
z370	1	0	0



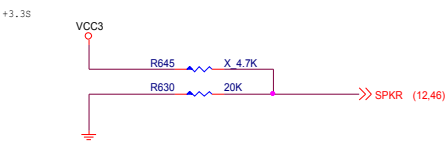


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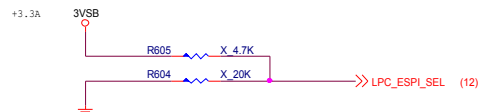


TOP Swap



Internal pull-down is disabled after PLTRST#

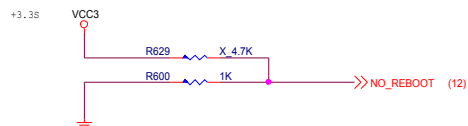
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

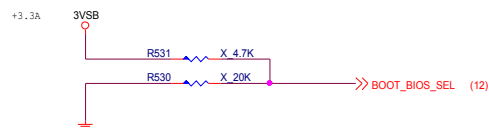
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

Boot BIOS

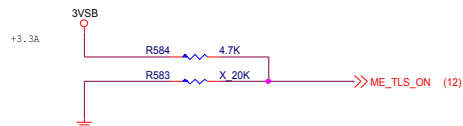


0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

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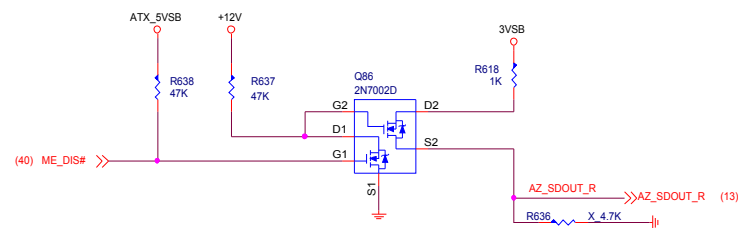
AMT and SBA with confidentiality



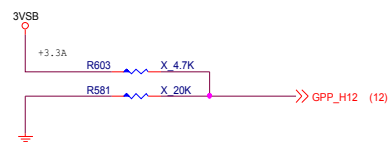
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



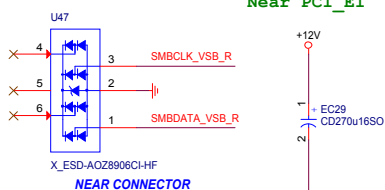
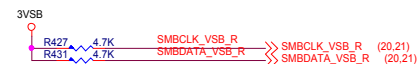
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST



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MS-7B49		
Size Custom	Document Description PCH-Strap	Rev 1.1
Date: Tuesday, August 08, 2017	Sheet 18 of 69	

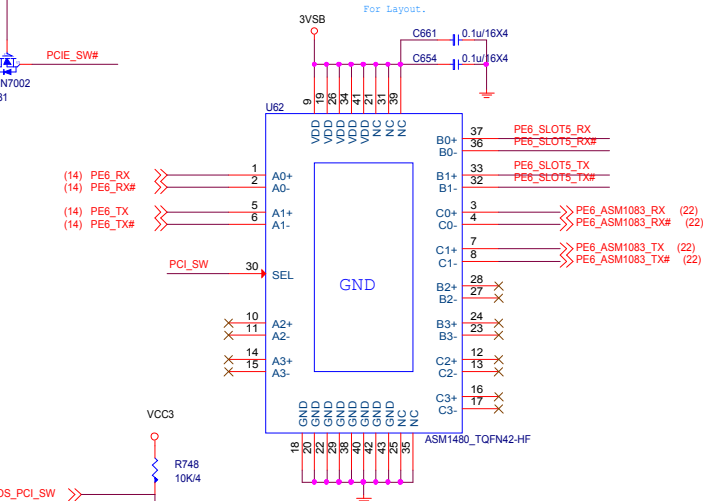
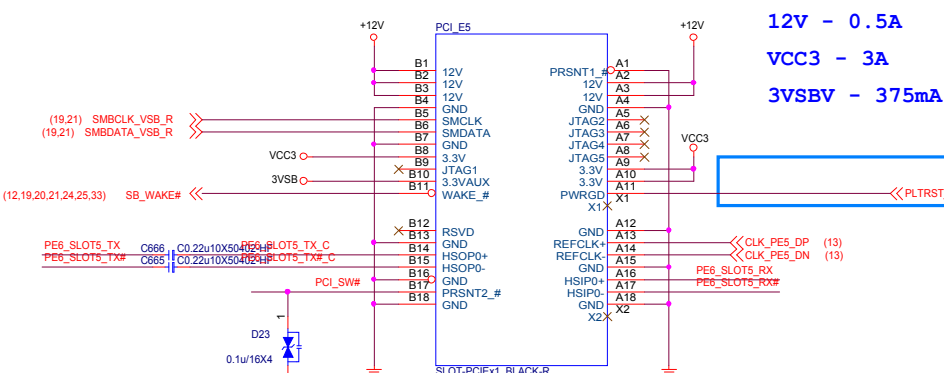
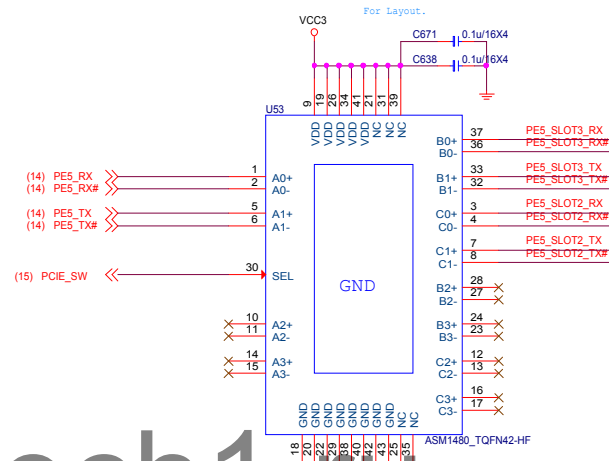
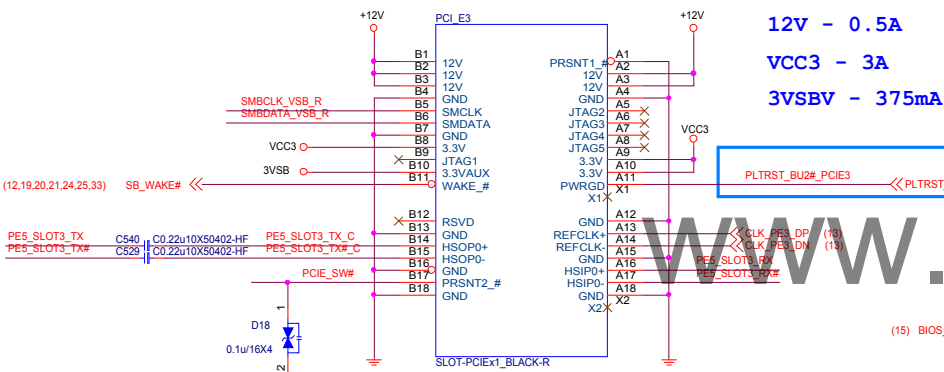
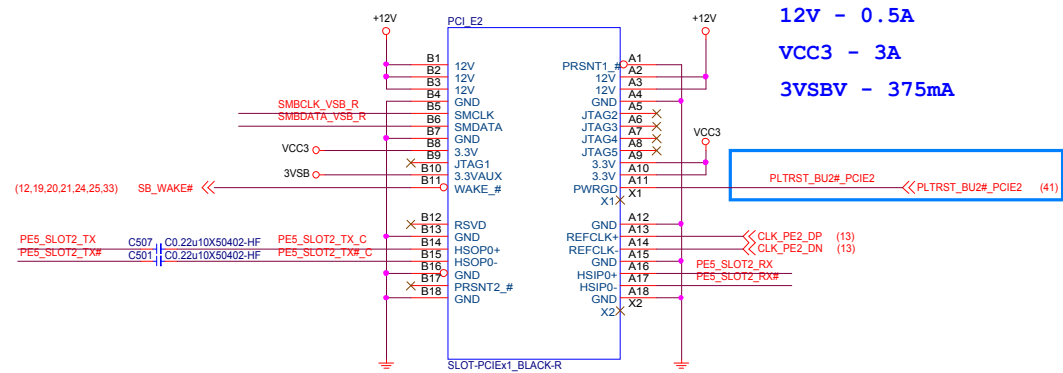
12V - 5.5A
VCC3 - 3A
3VSB - 375mA



Near PCI_E1

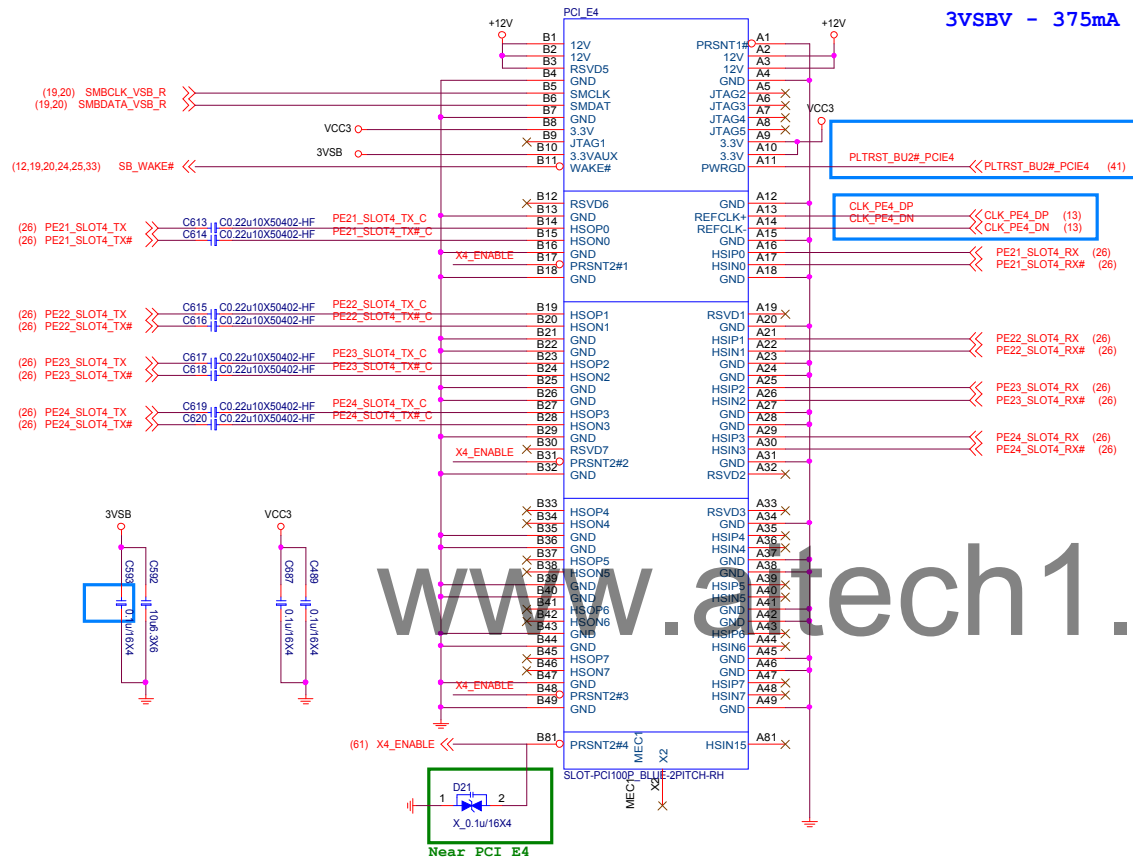
(12,20,21,24,25,33) SB_WAKE#



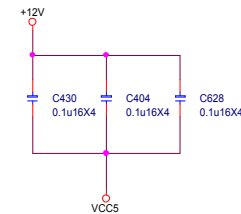
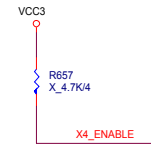
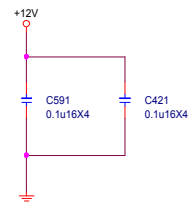
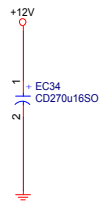


PCI Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



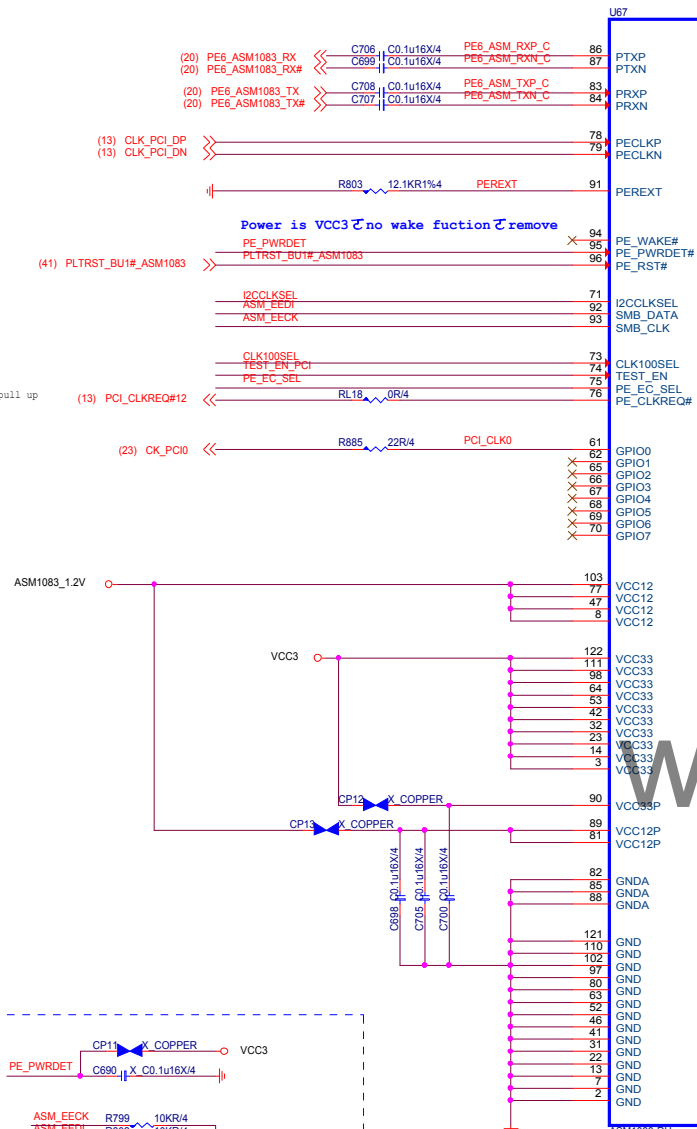
Near PCI_E4



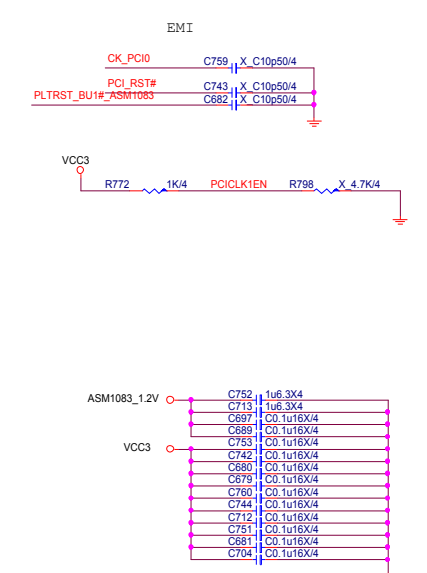
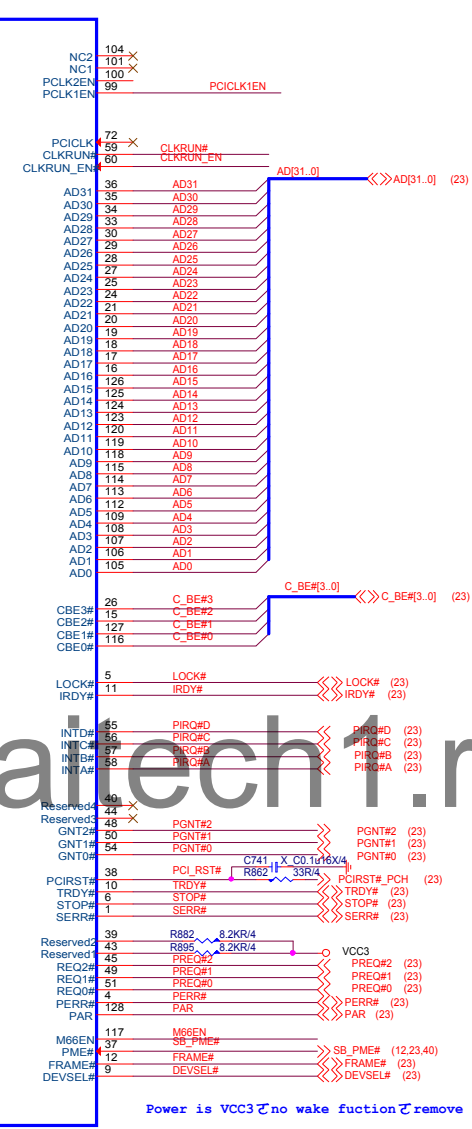
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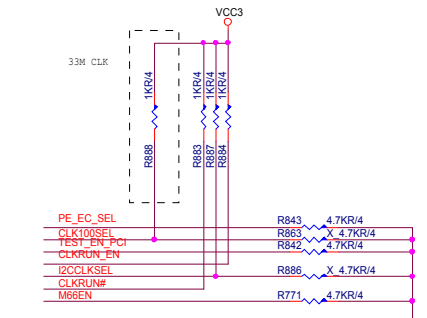
Size	Document Description	Rev
Custom	PCIE SLOT (X4)	1.1
Date: Tuesday, August 08, 2017	Sheet 21 of 69	



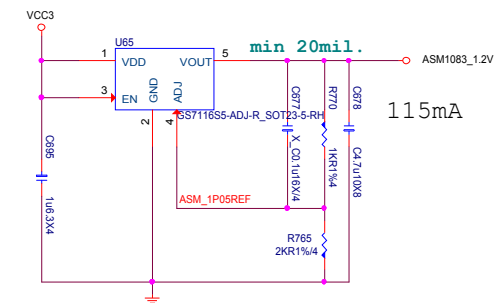
ASM1083



H/W Strapping



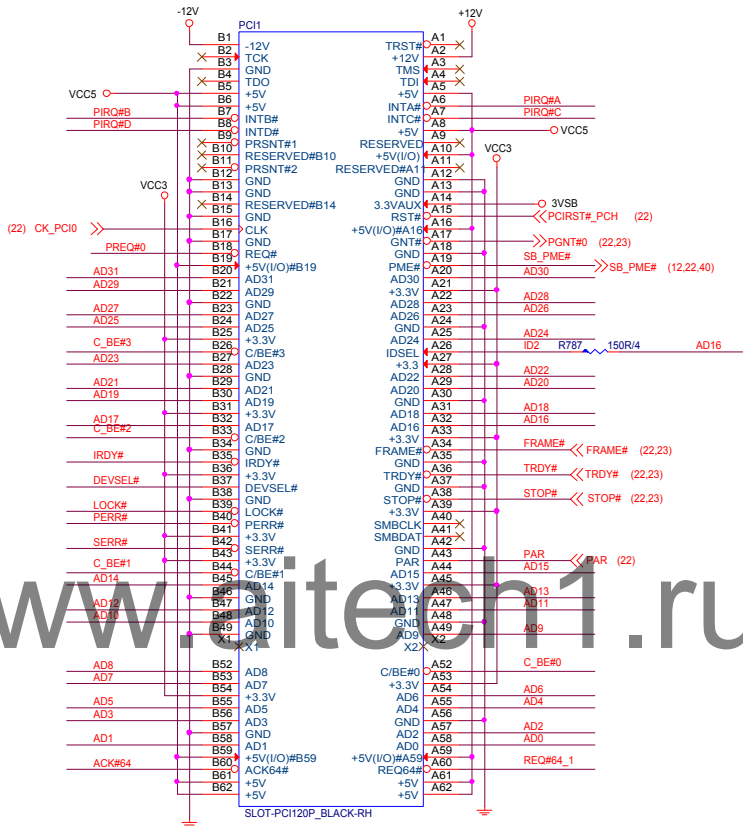
- PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
- CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
- TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
- CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
- I2CCLKSEL-
"H" is 135KHZ I2CCLK
"L" is 67.5KHZ I2CCLK



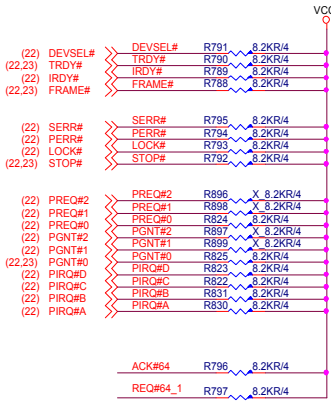
PCI

3.3Vaux:0.375*2=0.75A(wake)
0.02*2=0.04A(no wake)
VCC3 :7.6*2=15.2A
VCC5:5*2=10A
+12V:0.5*2=1A
-12V:0.1*2=0.2A

AD[31..0] <<> AD[31..0] (22)
C_BE#[3..0] <<> C_BE#[3..0] (22)

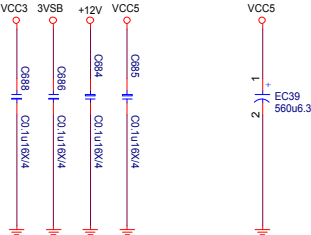


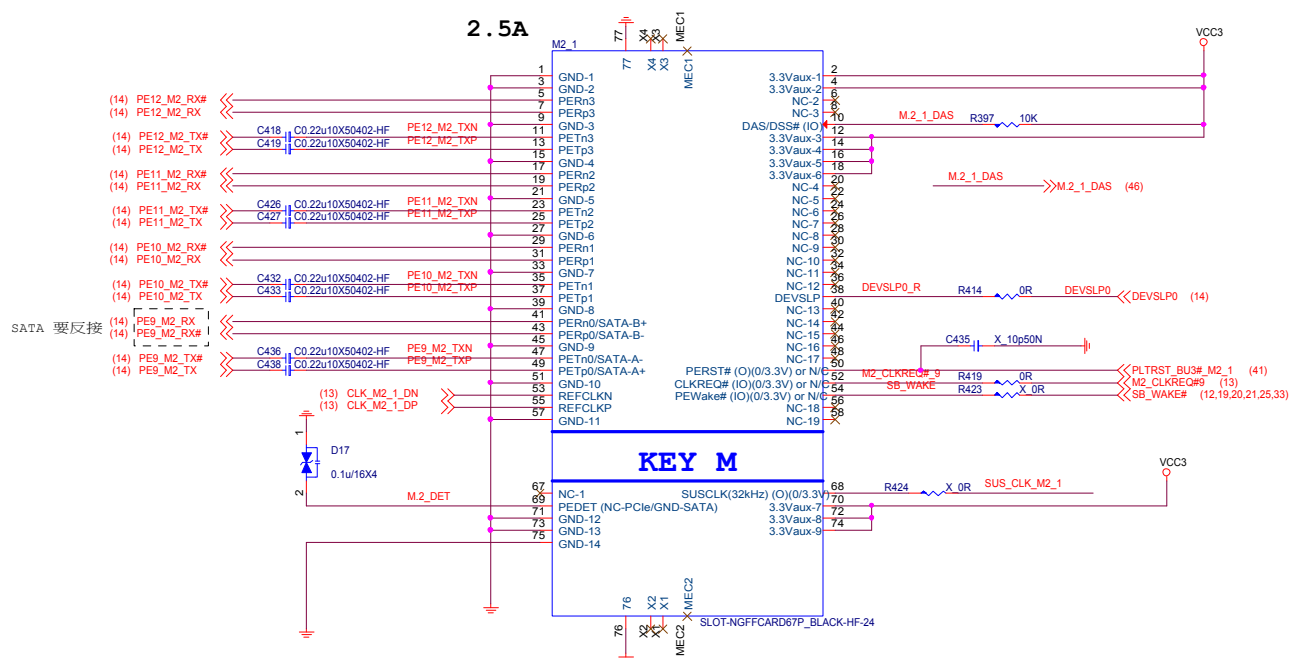
PCI PULL-UP / DOWN RESISTORS



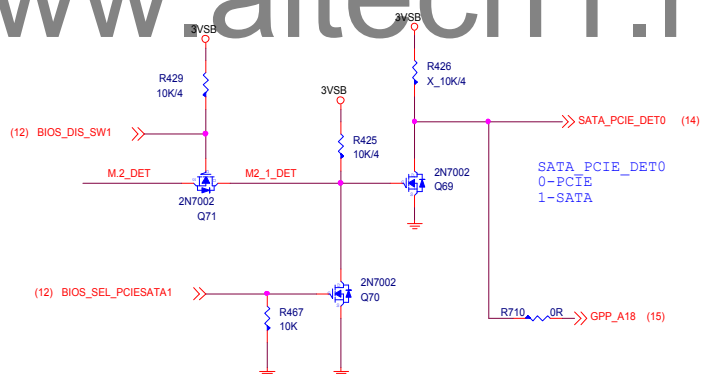
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

EMI:close pin

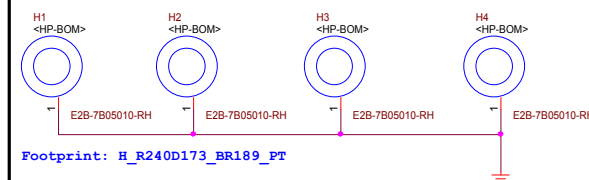




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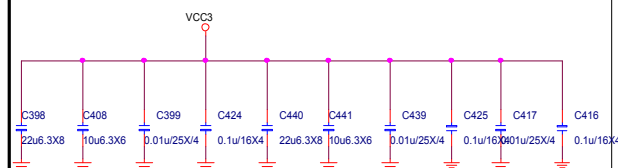
<i>BIOS_DIS_SW</i>	<i>BIOS_SEL_PCIESATA1</i>	<i>Mode</i>
<i>0</i>	<i>1</i>	<i>M2-SATA</i>
<i>0</i>	<i>0</i>	<i>M2-PCIE</i>
<i>GPI</i>	<i>GPI</i>	<i>AUTO</i>



Footprint: H R240D173 BR189 PT



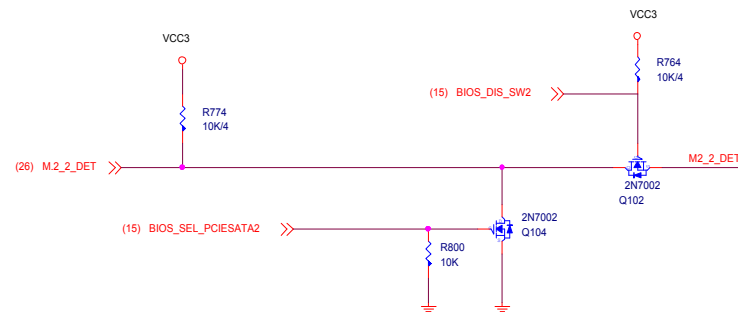
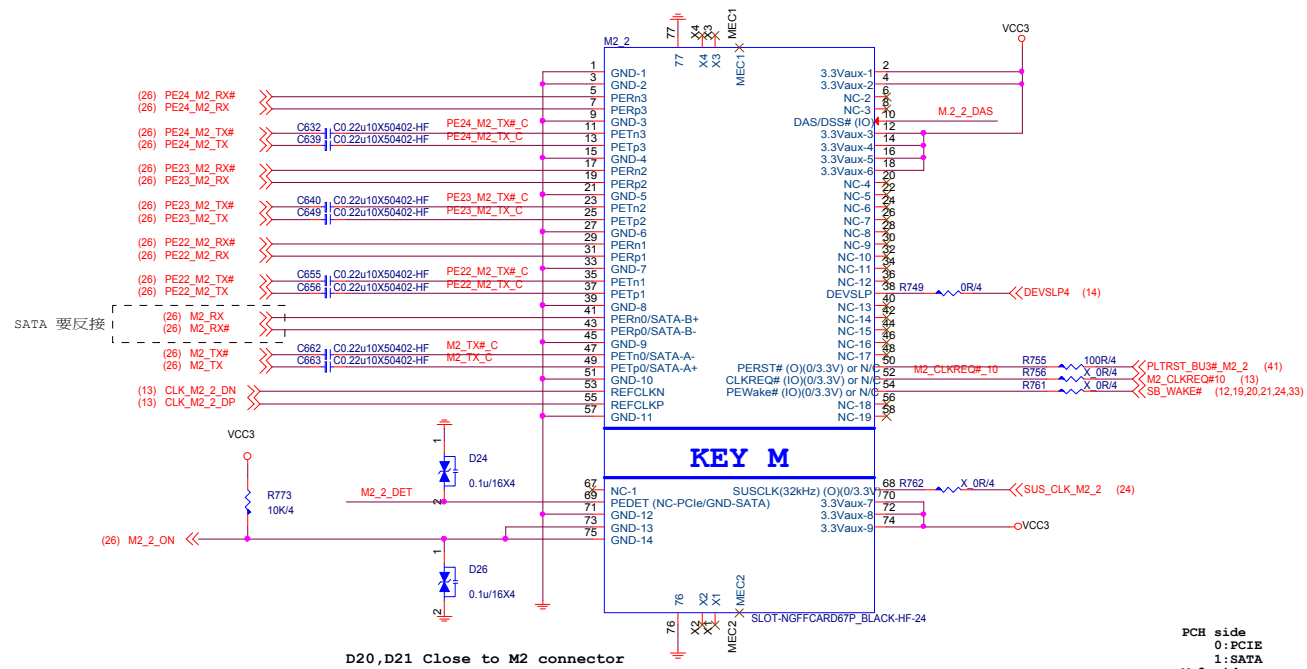
M:E2B-7B05020-A89
S:E2B-7B05020-H75



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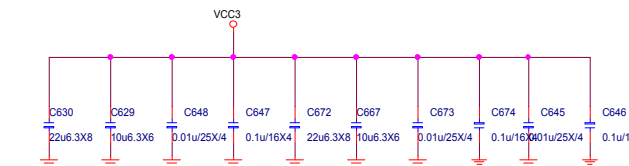
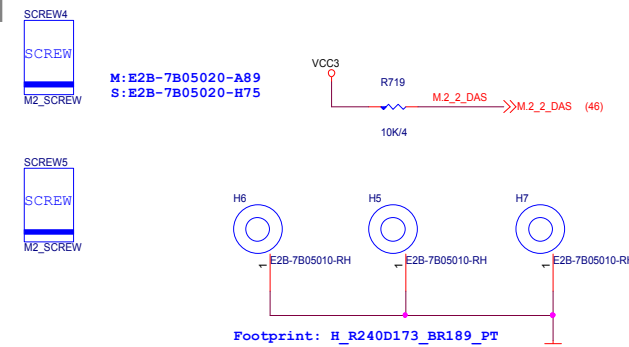
MS-7B49

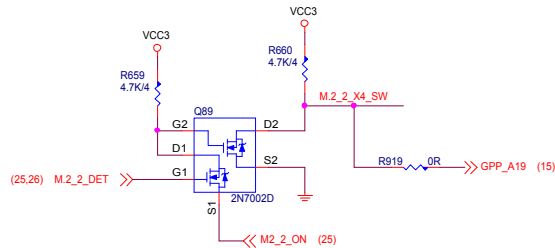
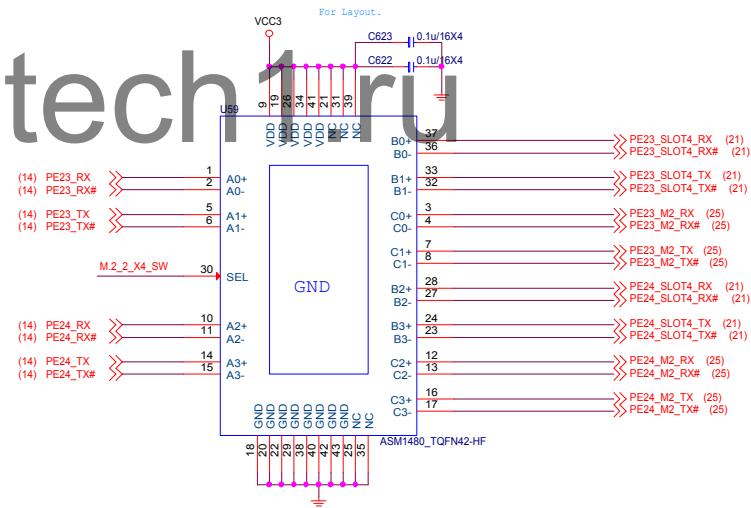
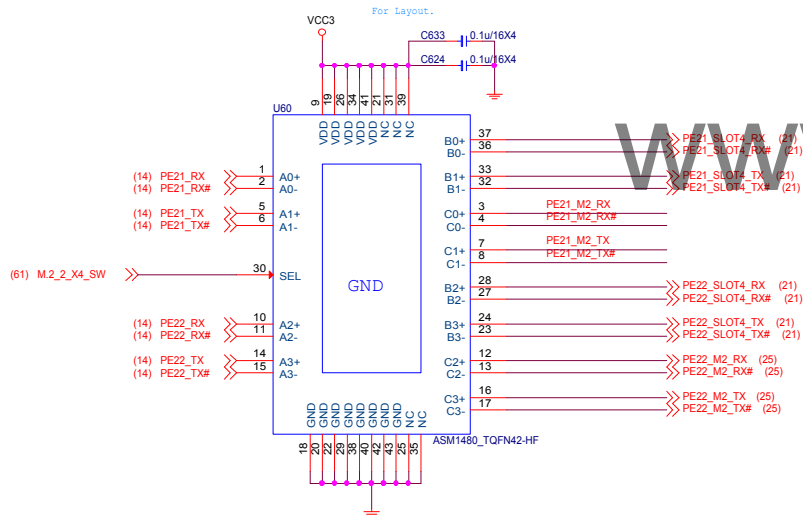
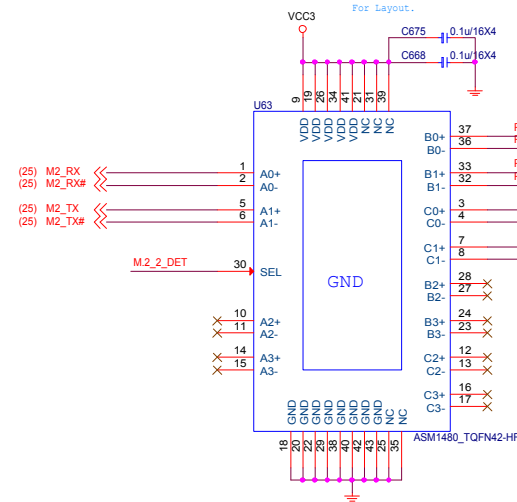
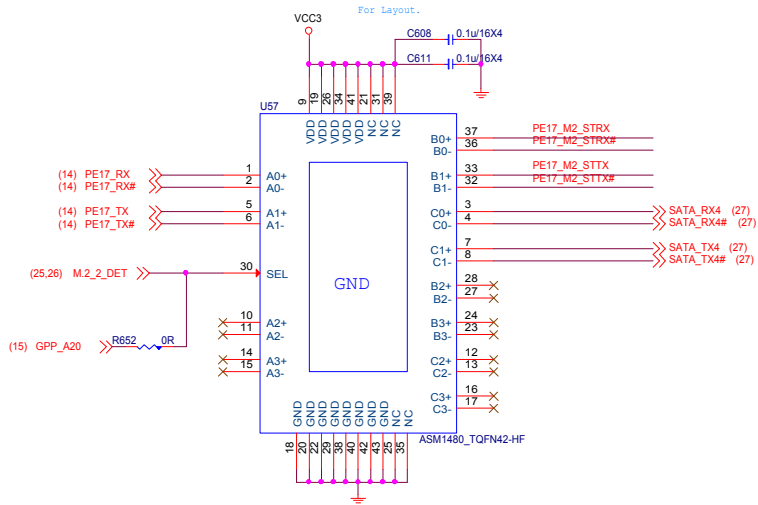
Size Custom	Document Description M.2-SLOT1	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 24 of 69



BIOS_MODE

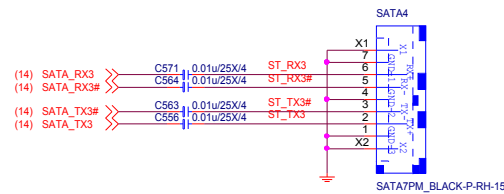
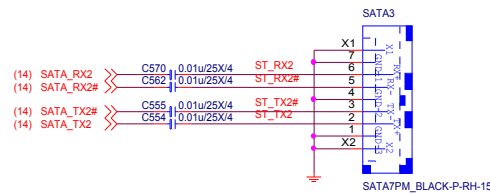
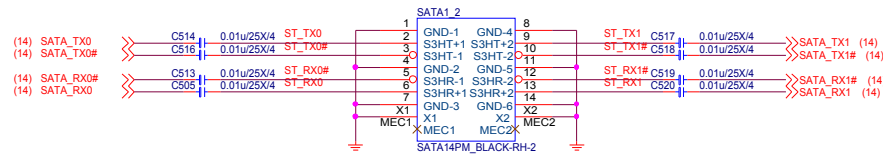
BIOS_DIS_SW2	BIOS_SEL_PCIESATA2	Mode
1	0	M2-PCIE
0	1	X4 SLOL-PCIE
GPI	GPI	GPI



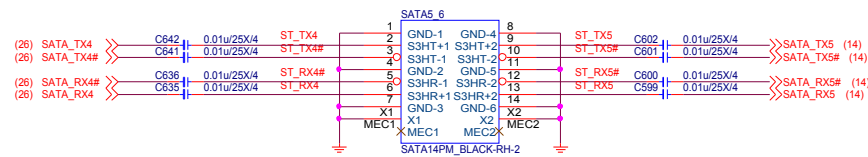


Default
M.2_2 PCIE
M.2_2 SATA

M2_2_ON	M.2_2_X4_SW	M.2 SATA	M.2 PCIE	X4 SLOT	SATA5
V	V	X	X	V	V
X	X	X	V	X	V
X	V	V	X	V	X



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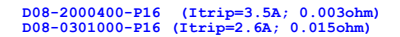
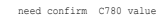
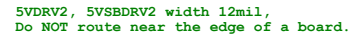


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MS-7B49

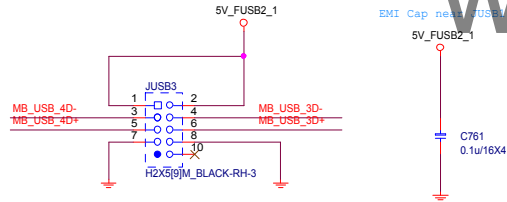
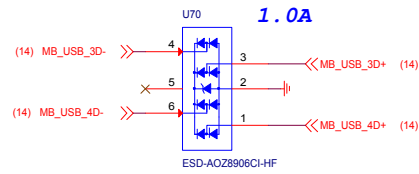
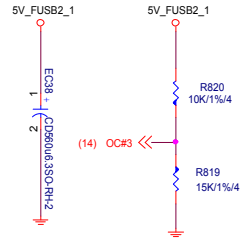
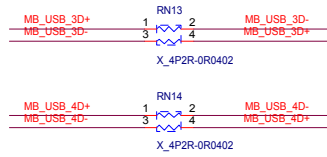
Size	Document Description	Rev
Custom	SATA Express/SATA Connector	1.1
Date: Tuesday, August 08, 2017	Sheet 27 of 69	

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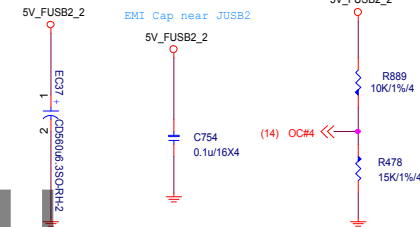
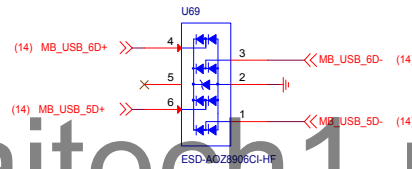
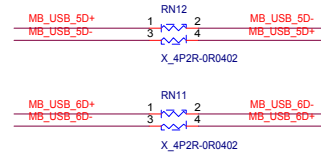


N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

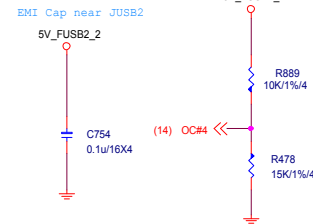
FRONT USB2.0 PORT 3,4



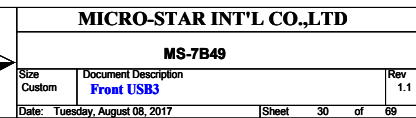
FRONT USB2.0 PORT 5,6



1.0A

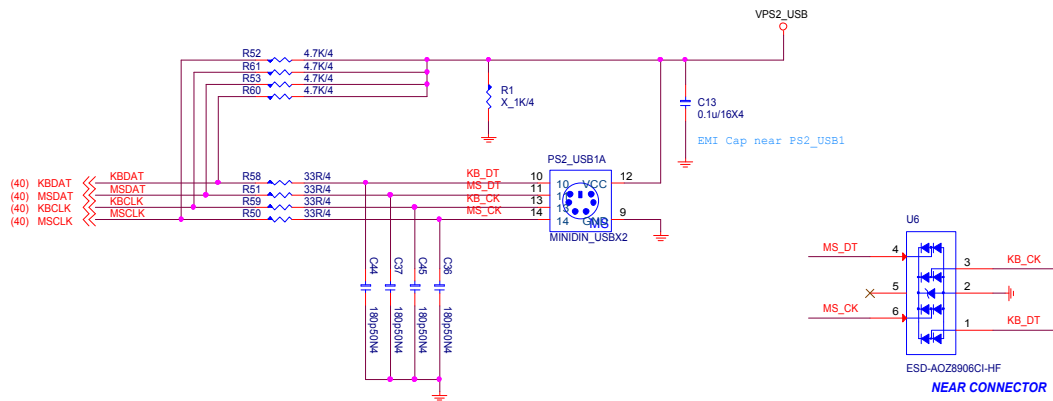


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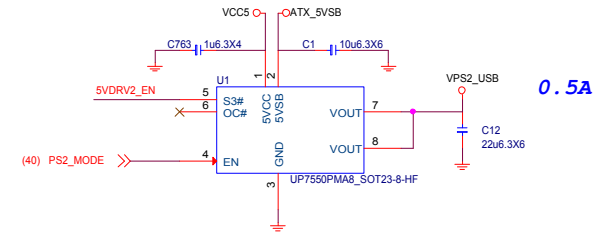


PS2 KEYBOARD & MOUSE CONNECTOR

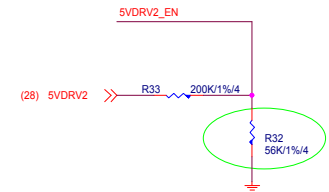
PS2 Connector



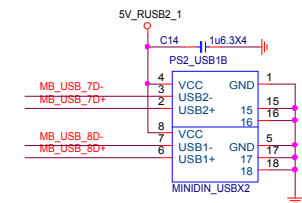
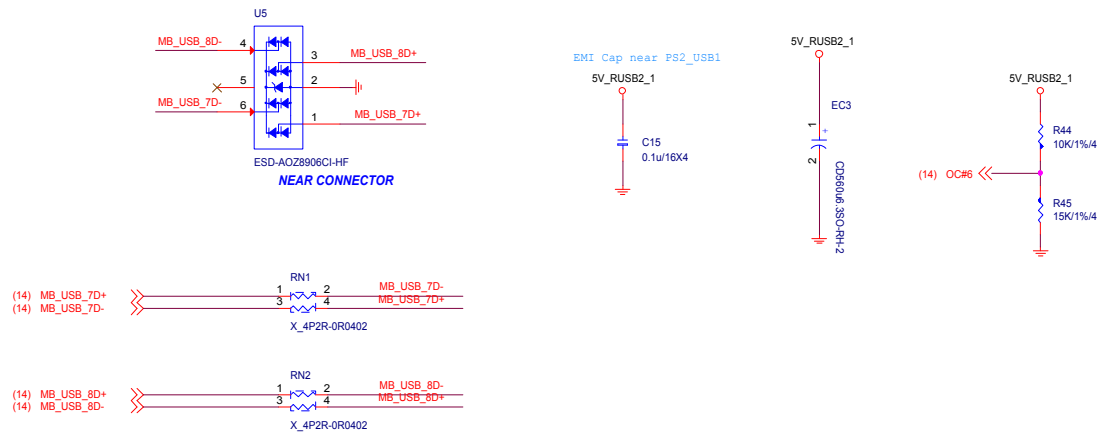
PS2 Power

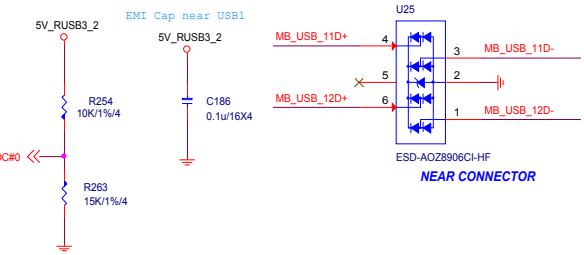
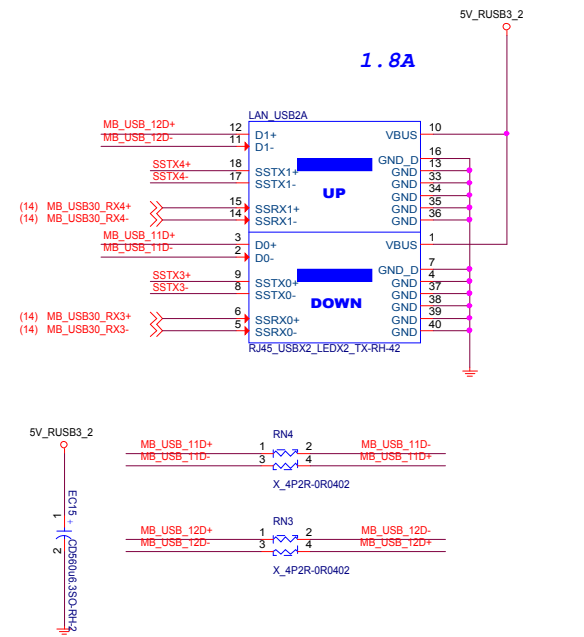
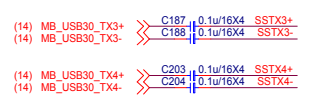
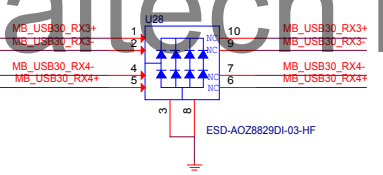
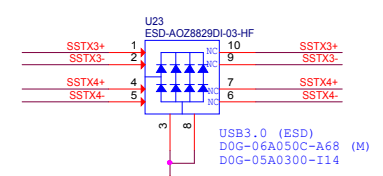
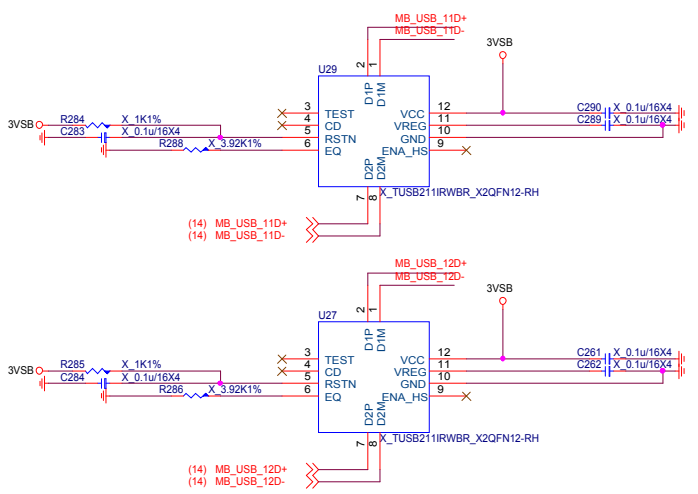
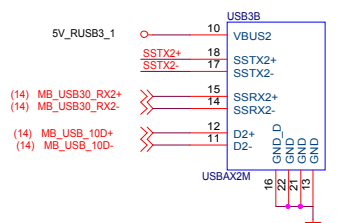
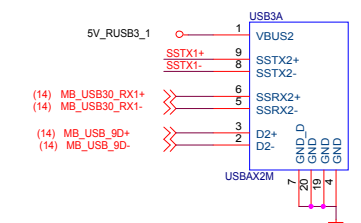
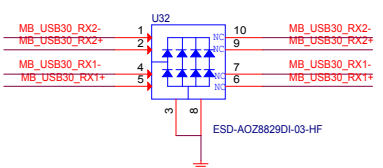
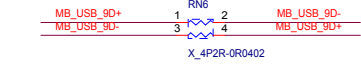
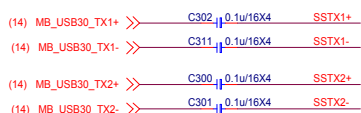
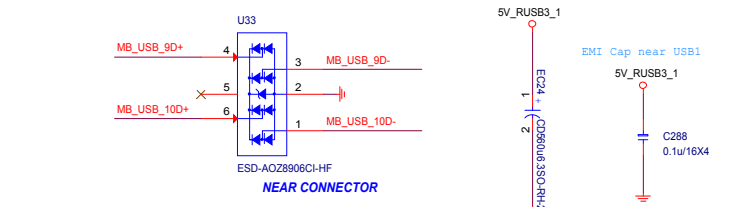


USB MODE

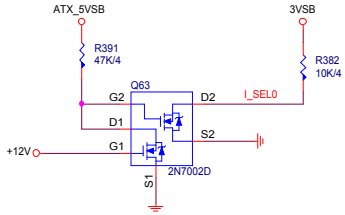


PS2_USB





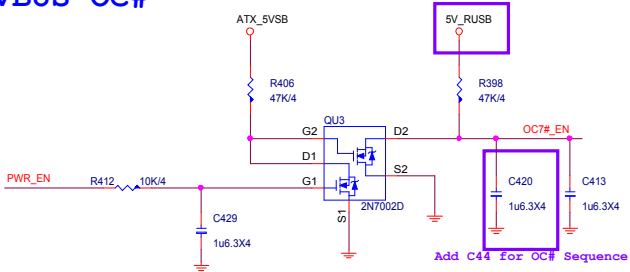
Current Mode



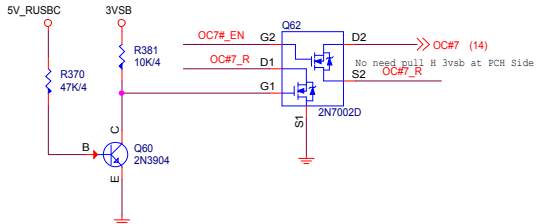
I_SELO: I_SEL1	
X	0
0	1
1	1

1.5A under S3 mode
3A under S0 mode

VBUS OC#

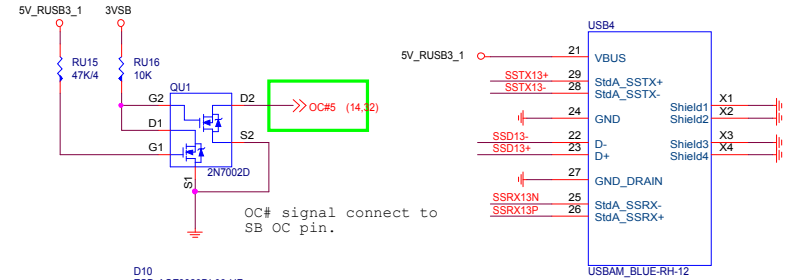


Add C44 for OC# Sequence

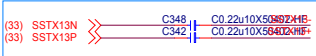
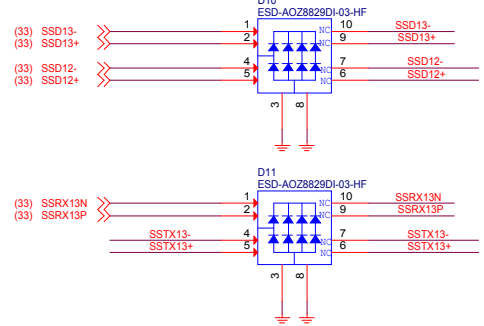


OC#7_EN
OC#7_R
OC#7_R

TYPE-A

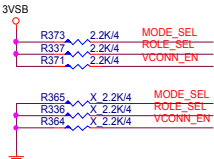


OC# signal connect to SB OC pin.



close to Connector USB4

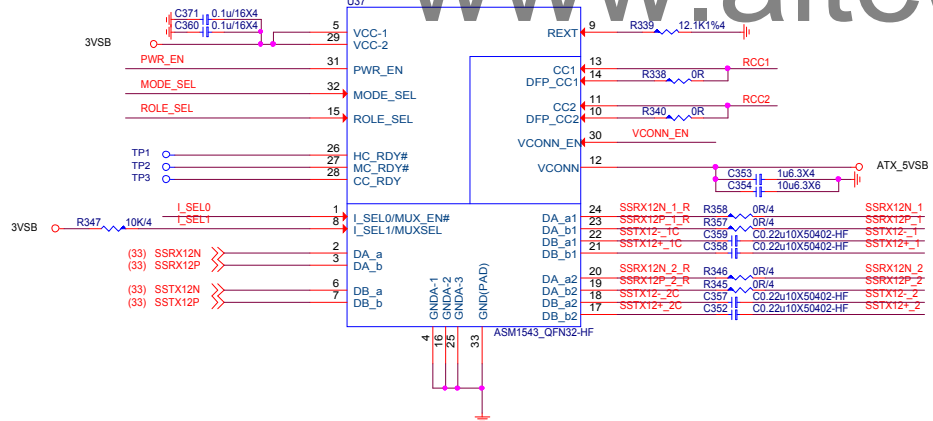
USB Type-C MUX with Configuration Channel (CC)



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

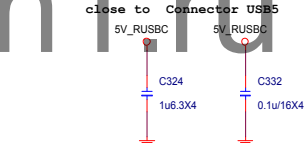
ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

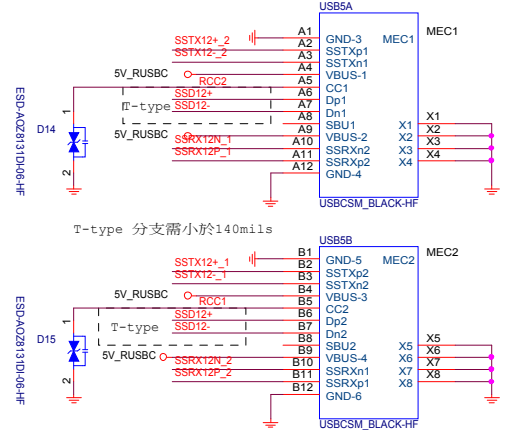
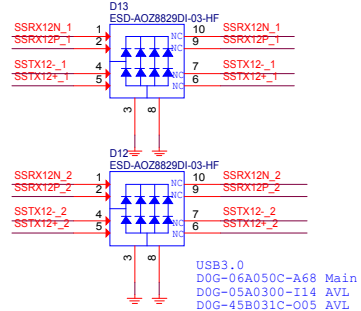


3 A min 80mil.

TYPE-C

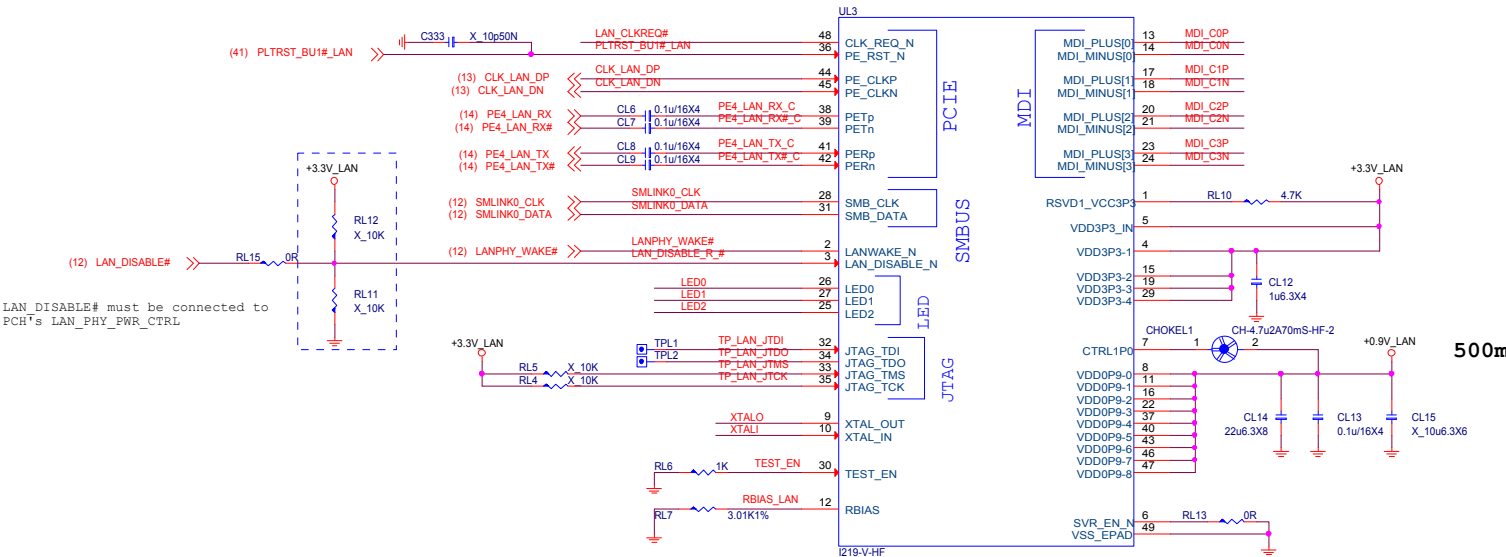


ESD Protection NEAR CONNECTOR



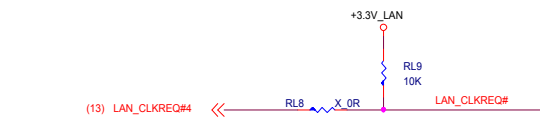
Intel Lan- I219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



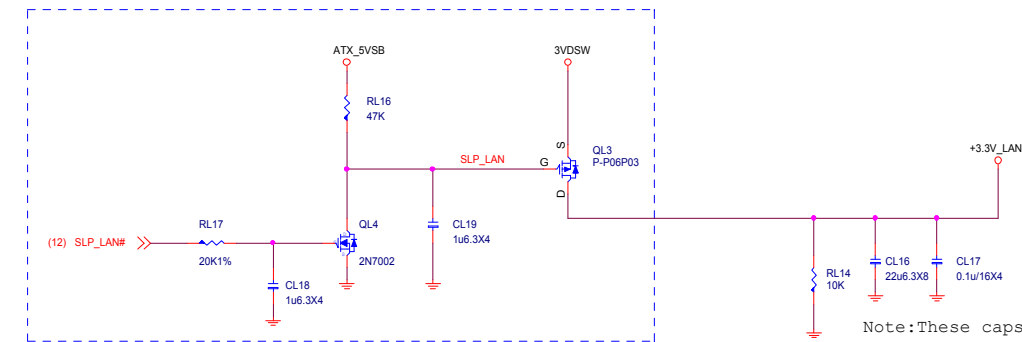
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



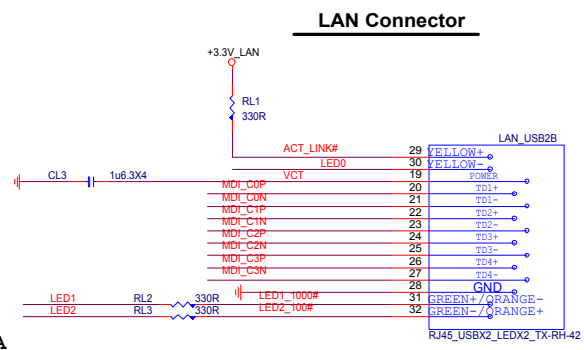
The 10Kohm pull-up resistor (RL8) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

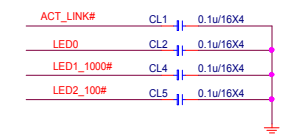


Note: These caps closed to PHY

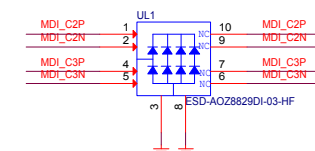
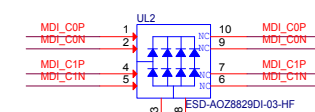
+3.3V LAN
I218: 132mA
I219: 542mW



For EMI



UL2&UL3 close to connector



Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue). Otherpairing combination is ok.

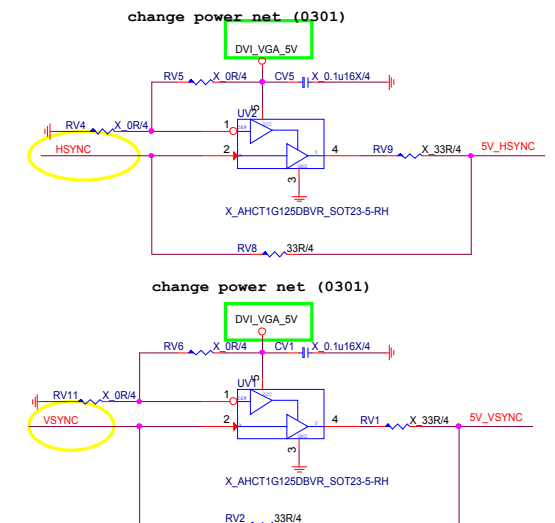
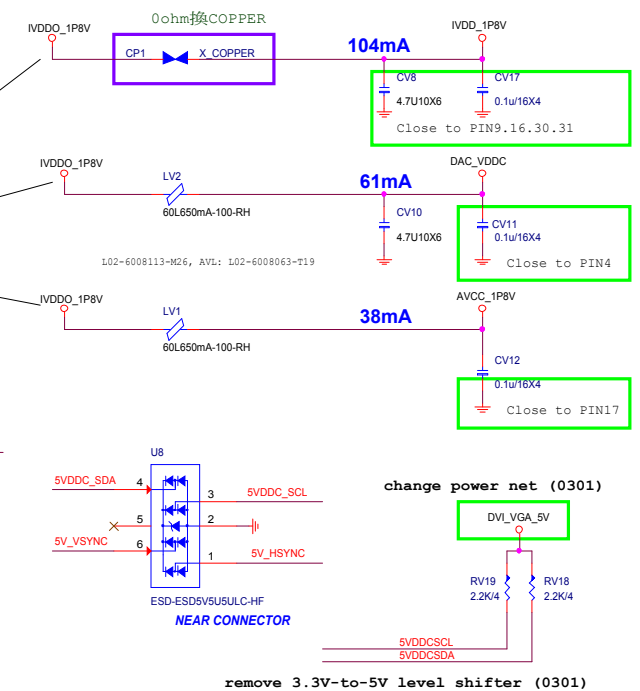
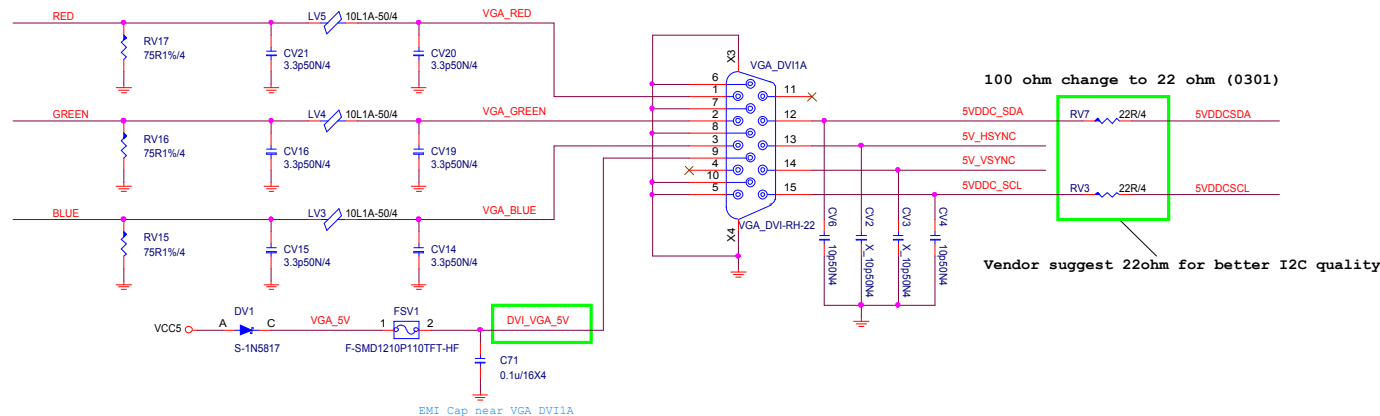
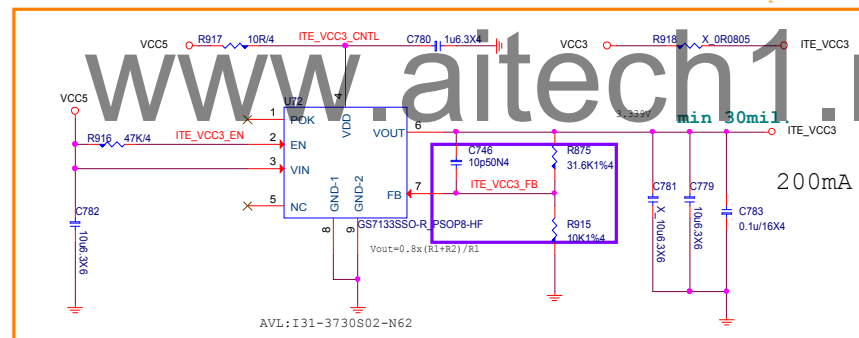
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MS-7B49			
Size	Document Description	Rev	
Custom	Intel Lan- i219	1.1	
Date:	Tuesday, August 08, 2017	Sheet	35 of 69

If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining

[illegible]

System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

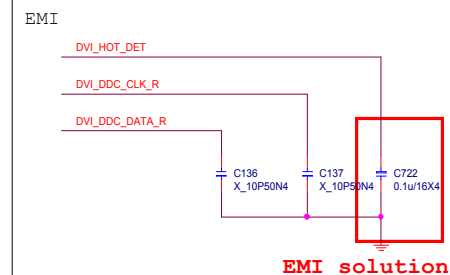
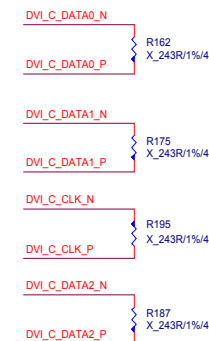
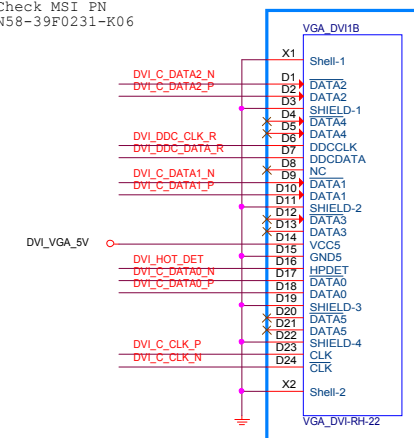
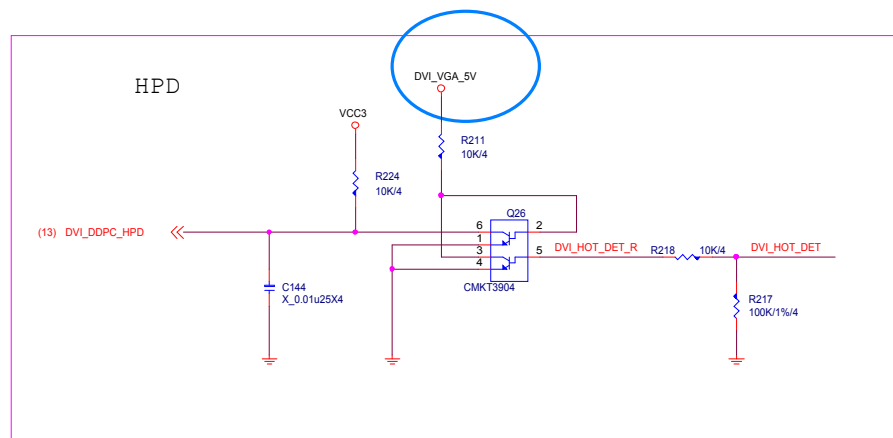
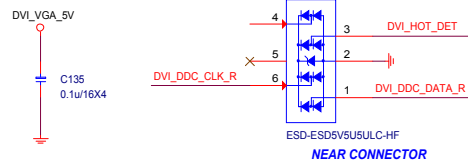
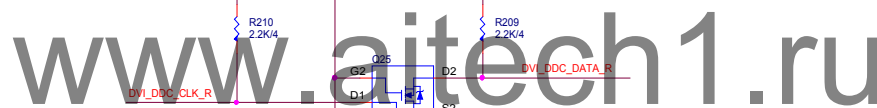
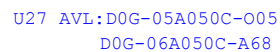
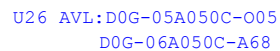


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MS-7B49

Size Custom	Document Description VGA - ITE6516	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 36 of 69

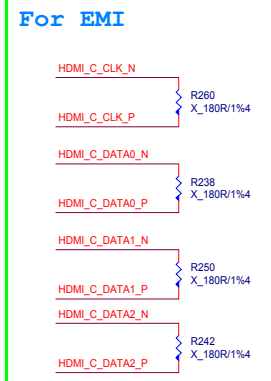
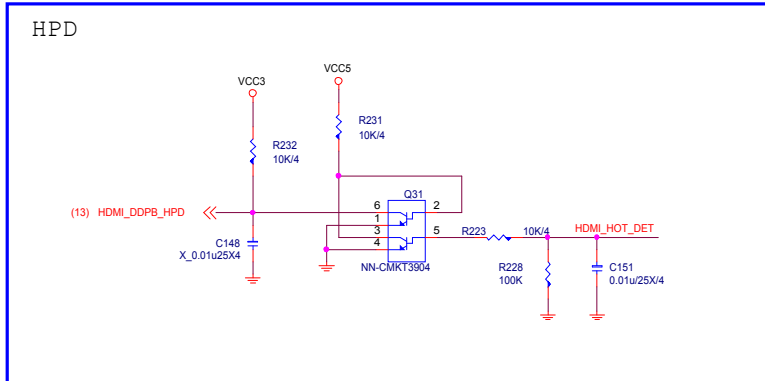
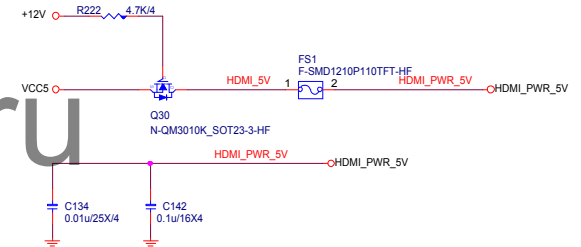
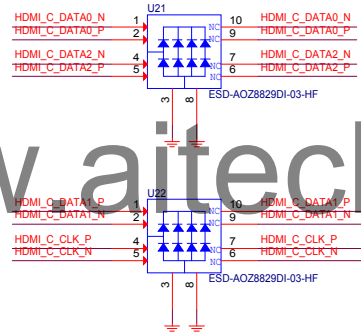
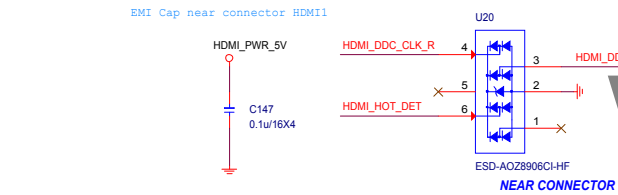
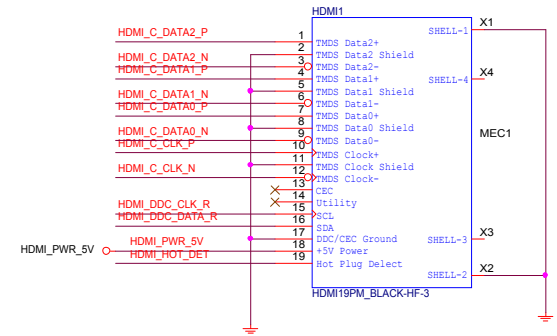
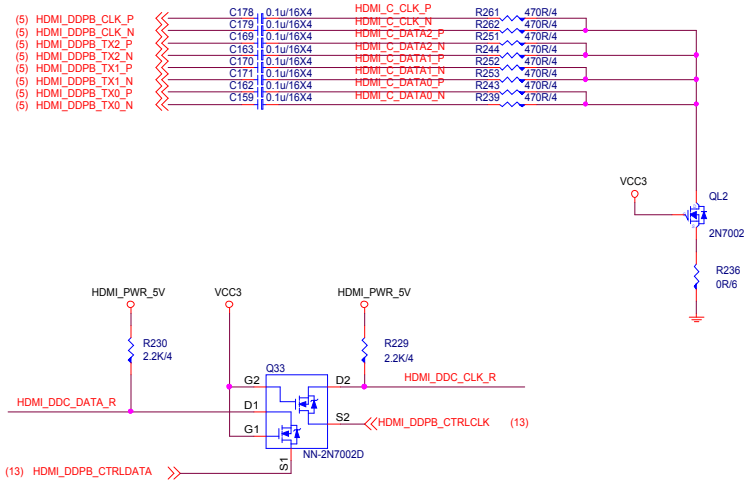
Check MSI PN
N58-39F0231-K06



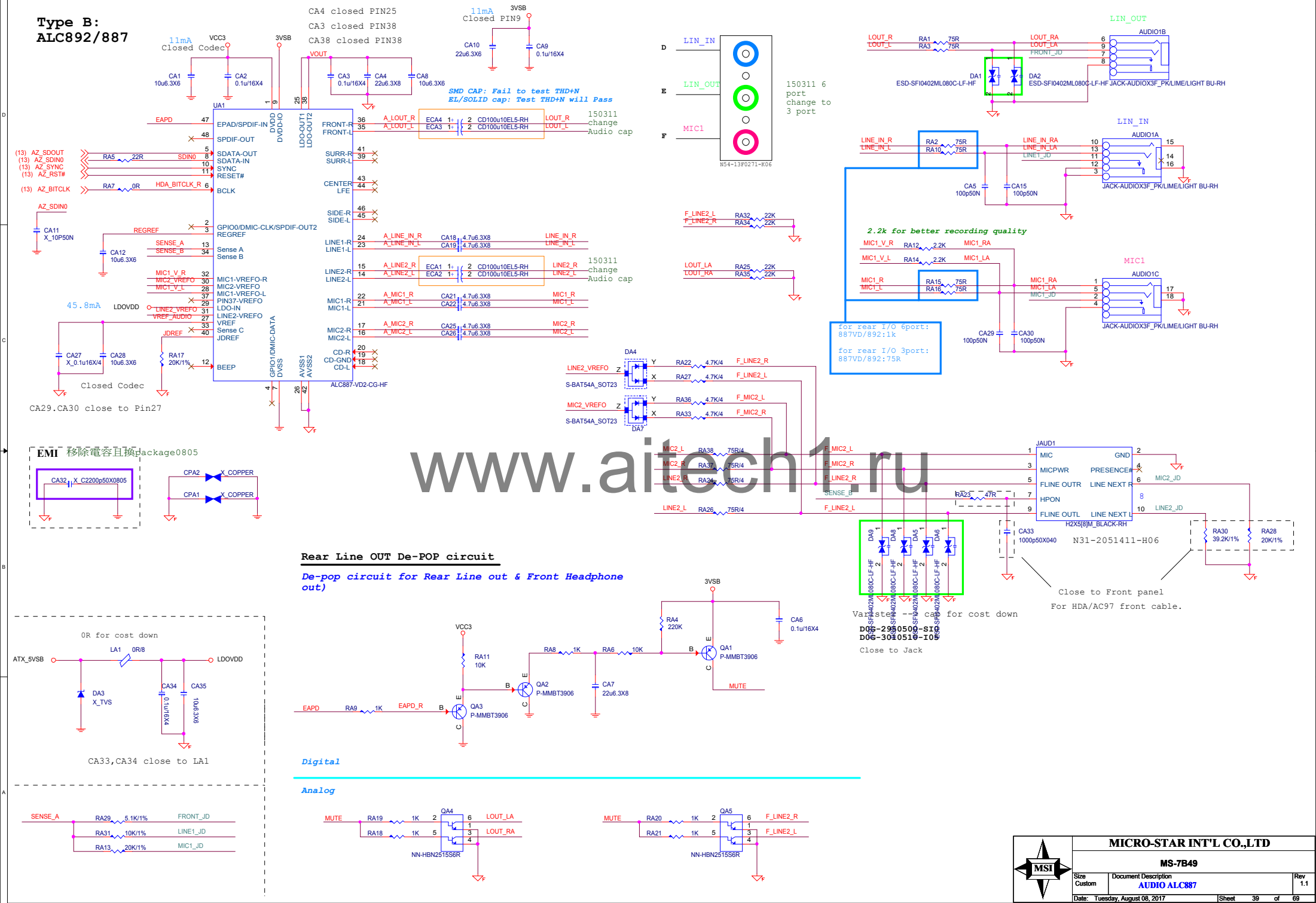
MS-7B49

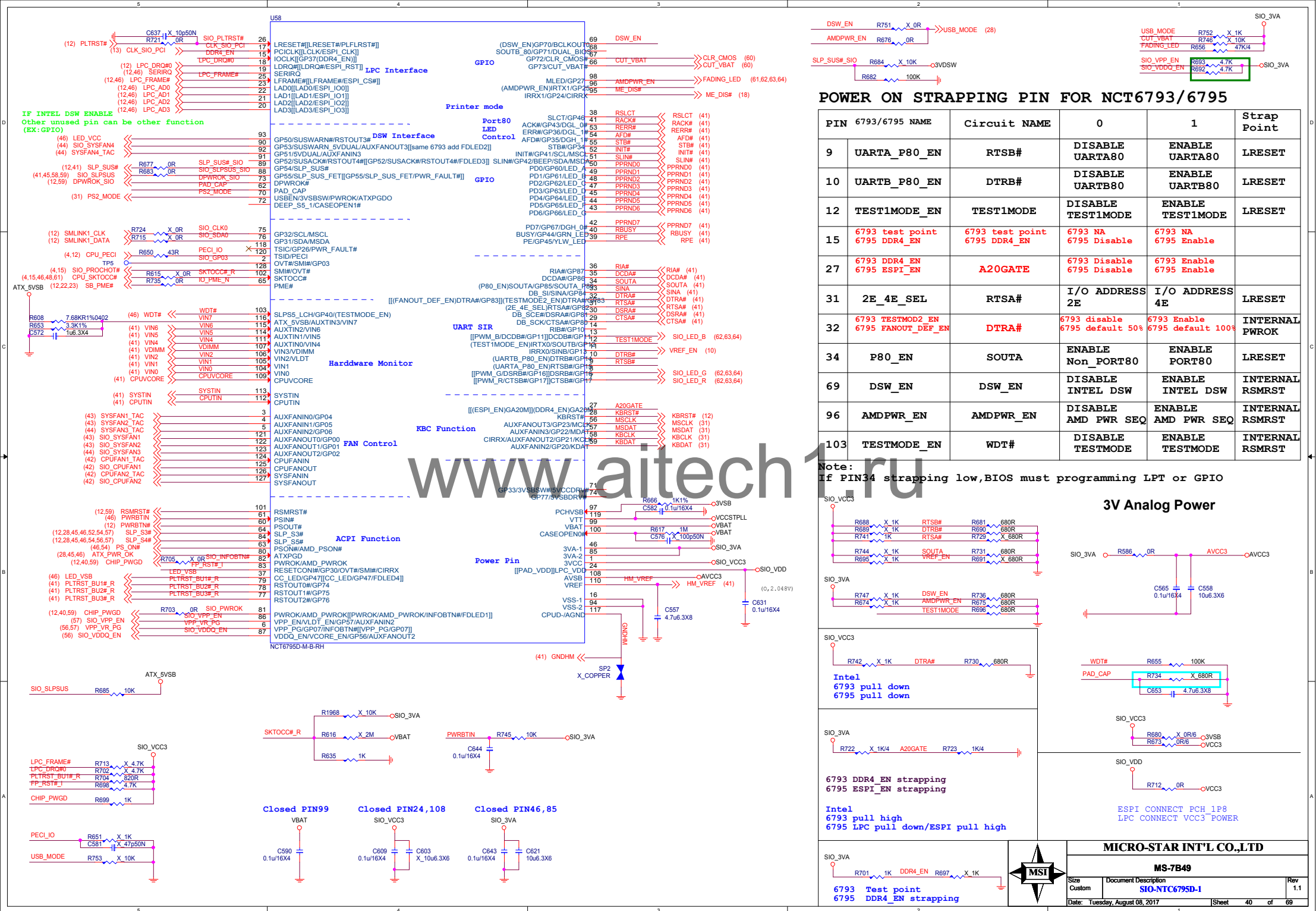
Size Custom	Document Description DVI Connector	Rev 1.
Date: Tuesday, August 08, 2017		Sheet 37 of 69

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



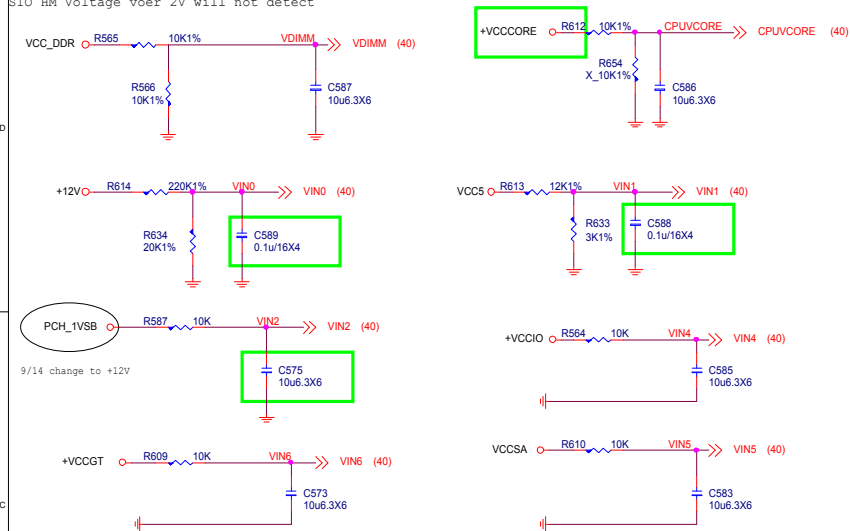
Type B: ALC892/887



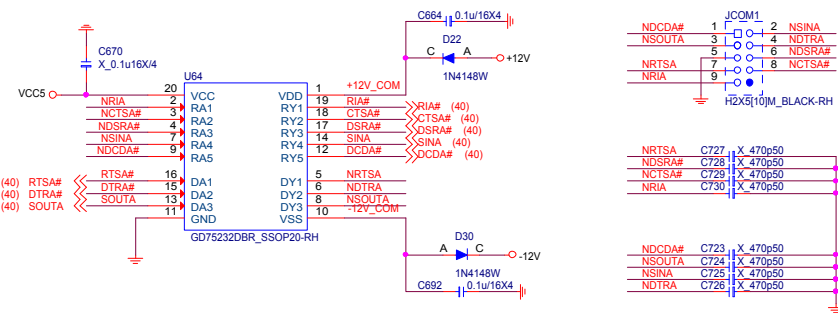
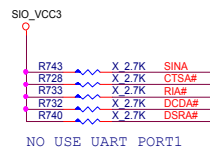


HW Monitor - Voltage

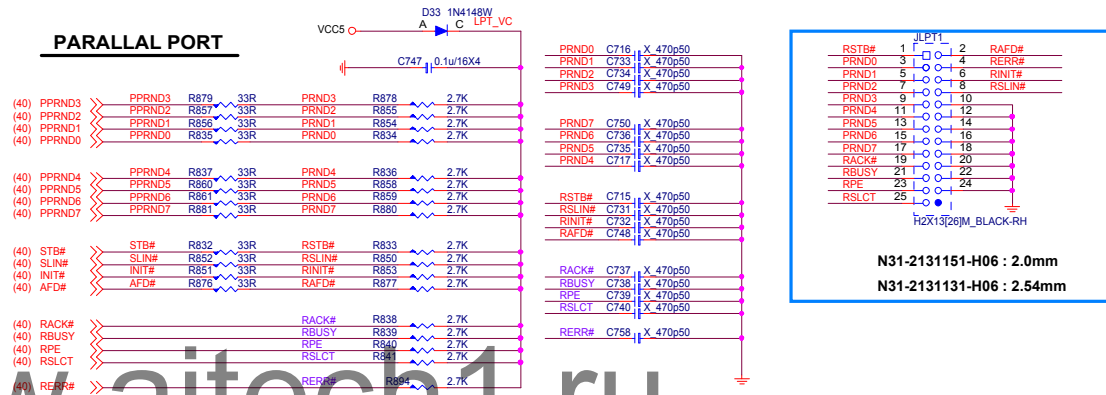
SIO HM Voltage voer 2V will not detect



SERIAL PORT 1

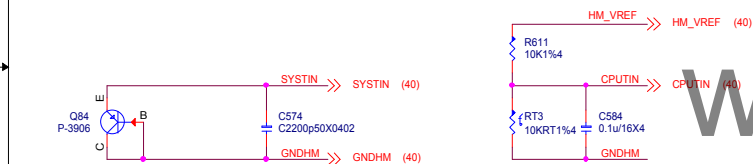


PARALLAL PORT



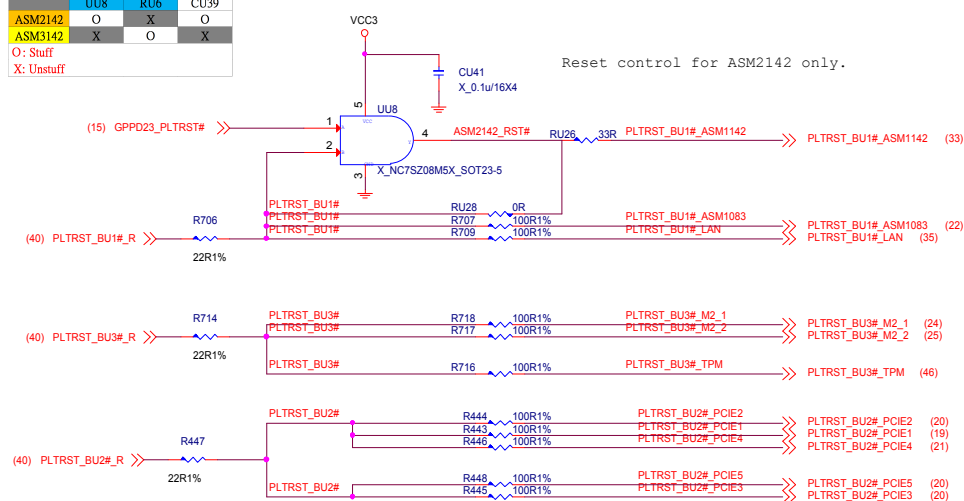
N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm

Thermal Monitor

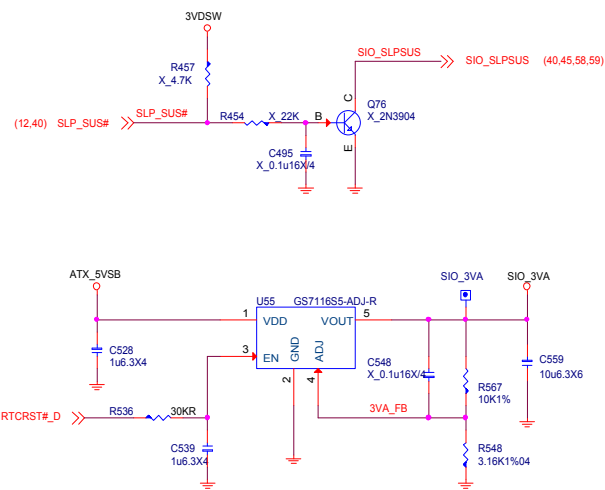


	U18	RU6	CU39
ASM2142	O	X	O
ASM3142	X	O	X
O: Stuff			
X: Unstuff			

Reset control for ASM2142 only.



SLP_SUS Co-lay circuit



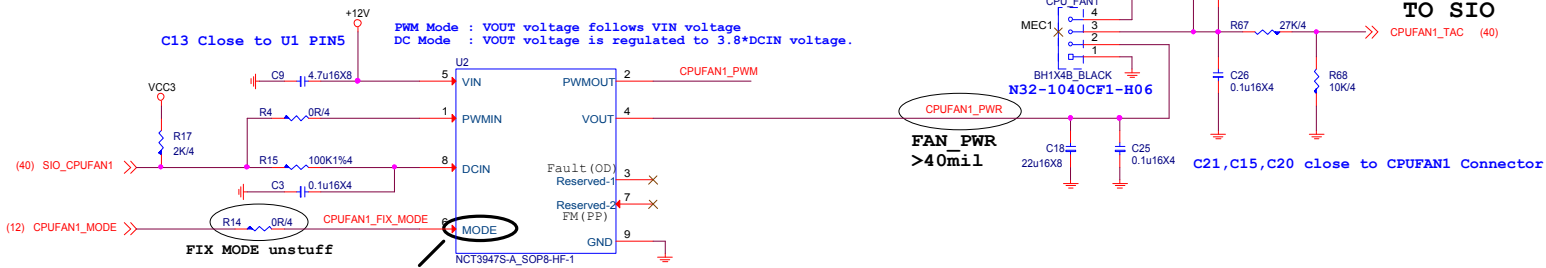
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MS-7B49

Size	Document Description	Rev
Custom	SIO-NTC6795D-2	1.1
Date: Tuesday, August 08, 2017	Sheet 41 of 69	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

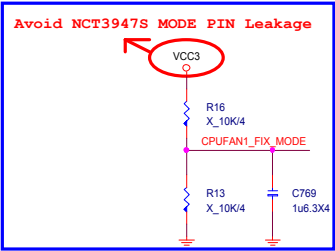
- 1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2. GPIO可以由BIOS切換 PWM/DC MODE
- 3. OCF拉回GPIO給BIOS認
- 4. PWM OR DC FAN拉回GPIO給BIOS認
- 5. FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化



GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

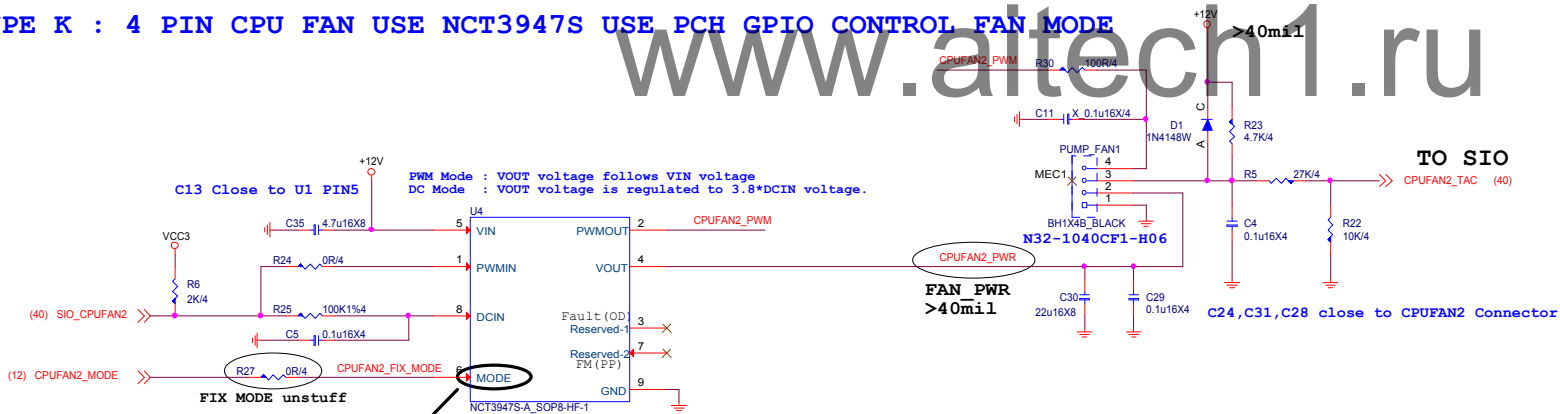
Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

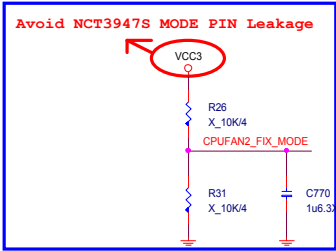
www.altech1.ru



GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

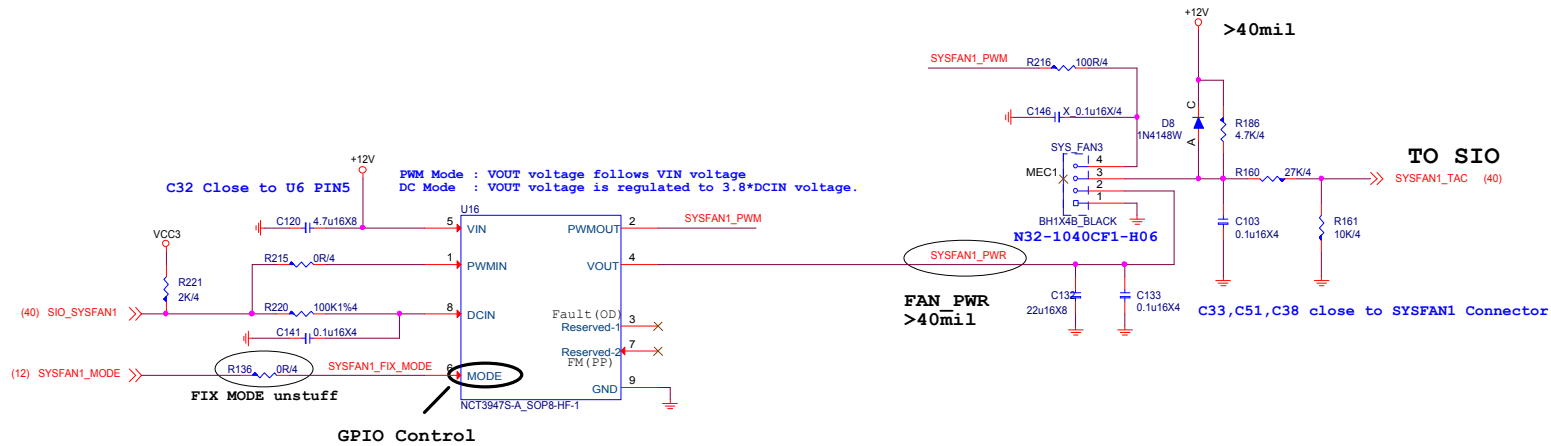
Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

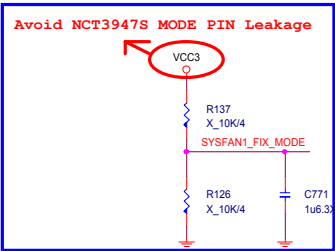
- 1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
- 2. FAULT : USE FAULT PIN Triger OVT/OCF Protection, LOW Atcive (Reserve NEW IC)
- 3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

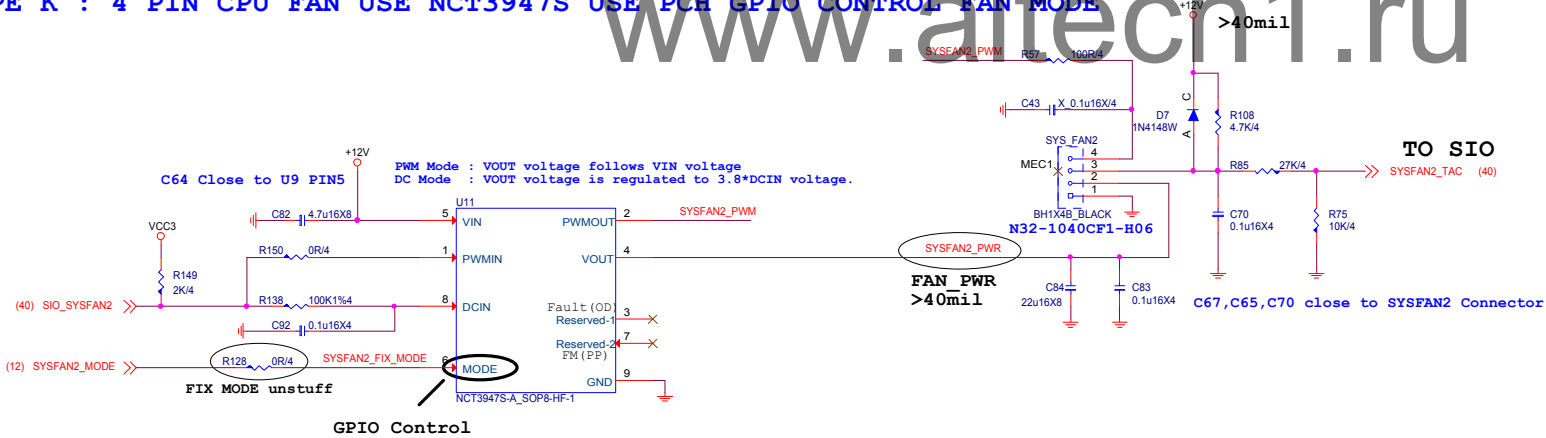
Default Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

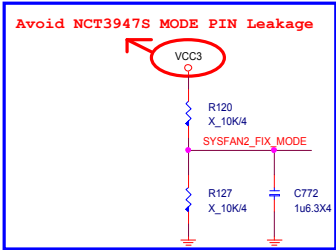
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

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	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

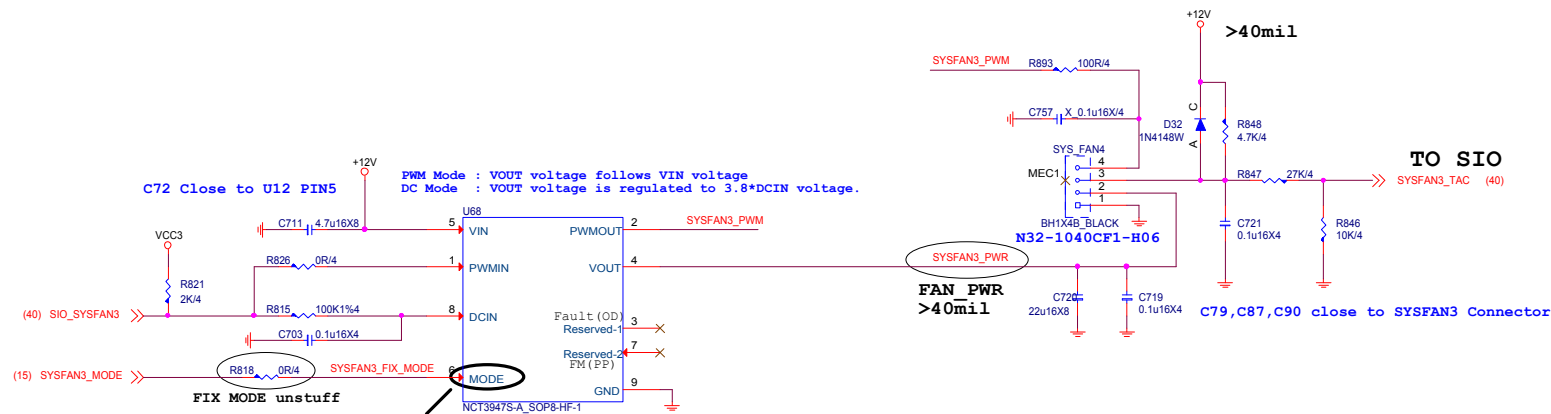


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MS-7B49

Size	Document Description	Rev
Custom	SYSTEM FAN 1/2	1.1
Date:	Tuesday, August 08, 2017	Sheet 43 of 69

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

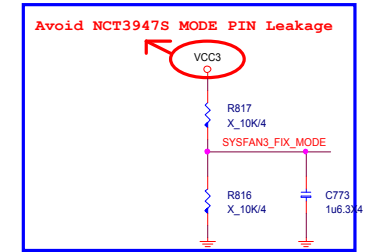


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

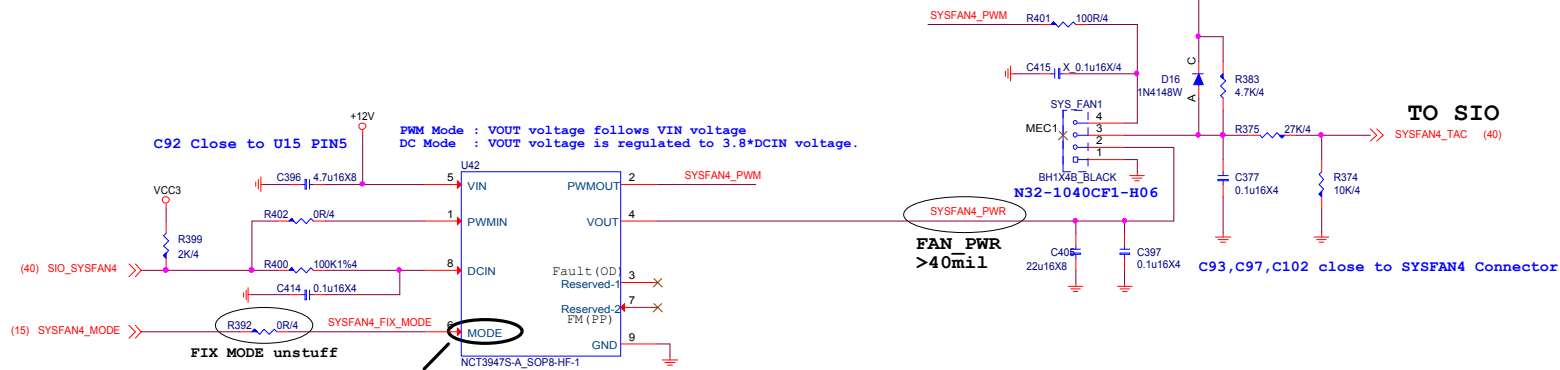
Internall pull up 1.65V



Reserver For FIX DC or PWM MODE USE By PM SPEC

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TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

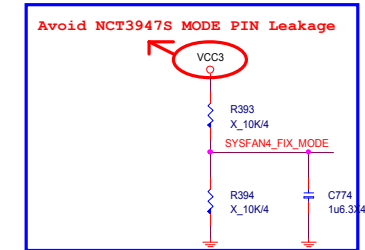


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V



Reserver For FIX DC or PWM MODE USE By PM SPEC

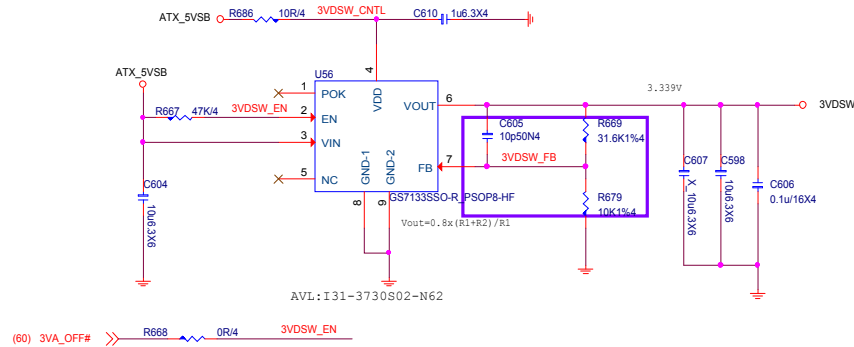


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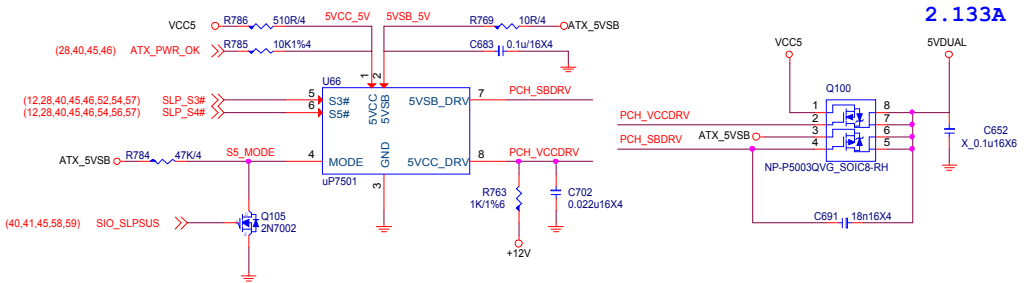
Size	Document Description	Rev
Custom	SYSTEM FAN 3/4	1.1
Date:	Tuesday, August 08, 2017	Sheet 44 of 69

3VDSW

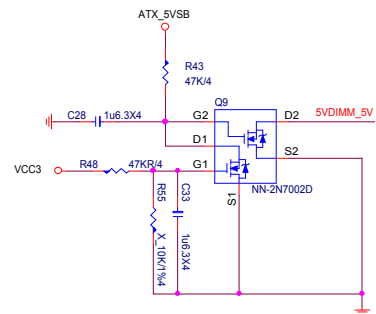
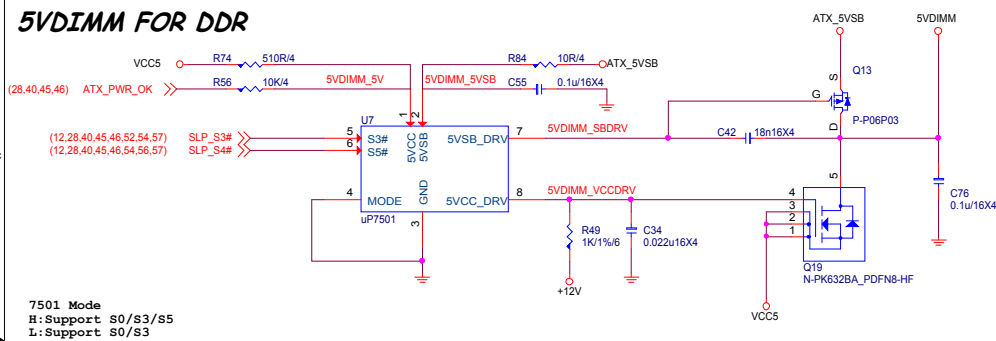


5VDUAL

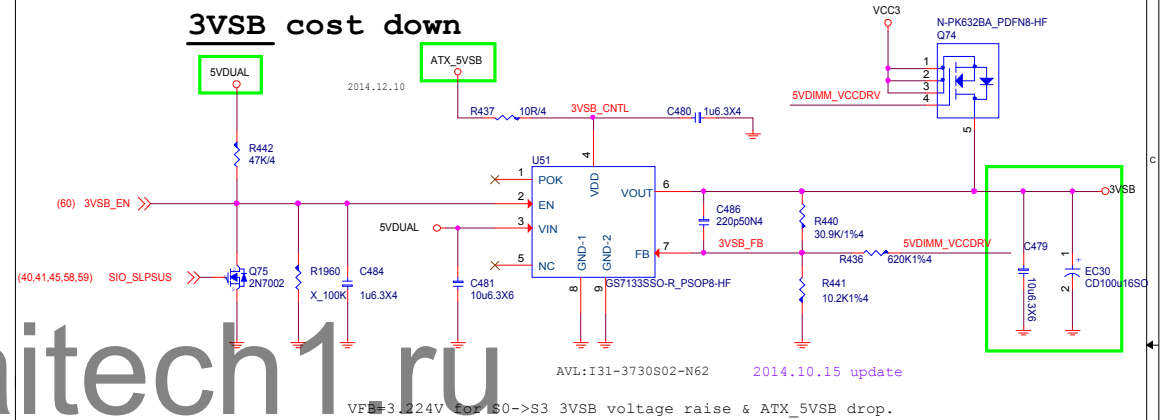
5VDUAL is power source of 1P0SB



5VDIMM FOR DDR



3VSB cost down



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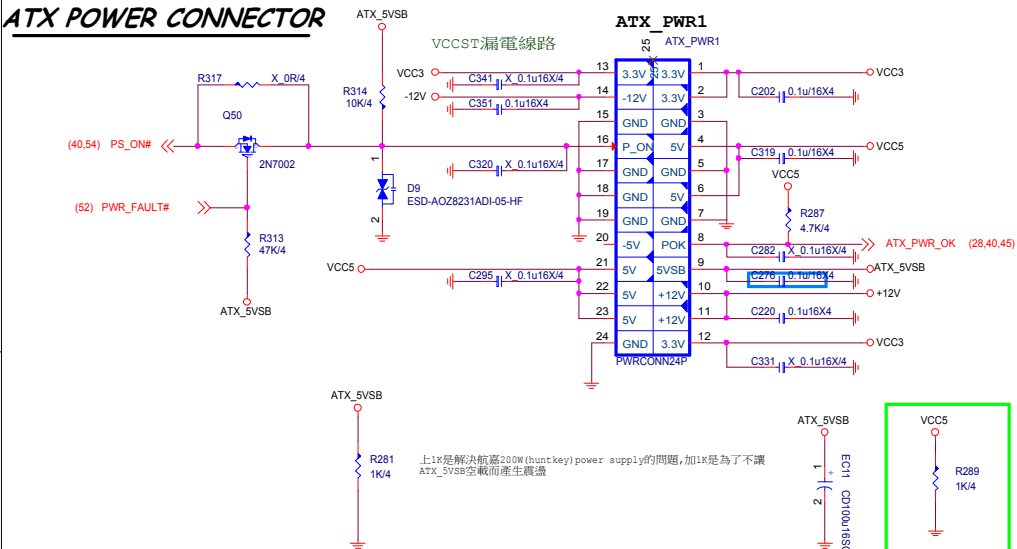


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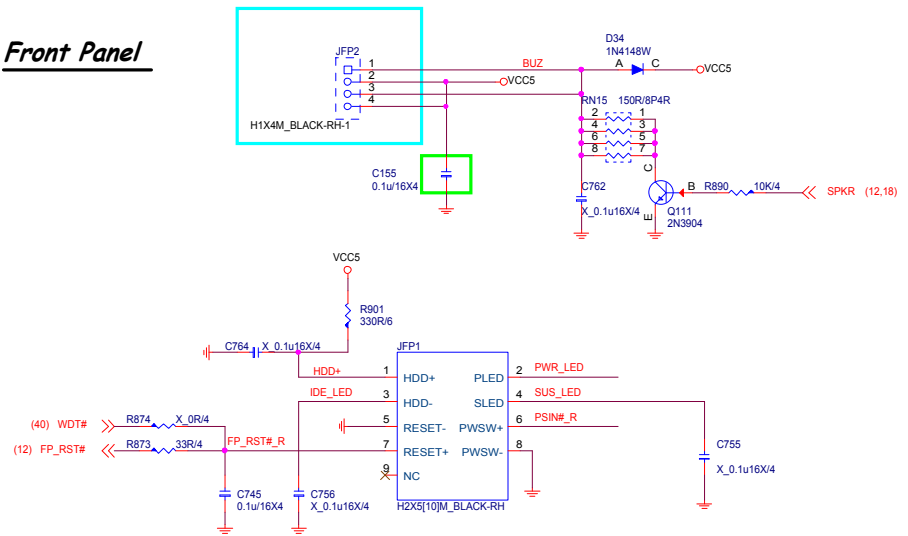
MS-7B49

Size	Document Description	Rev
Custom	ACPI UPI	1.1
Date: Tuesday, August 08, 2017	Sheet 45 of 69	

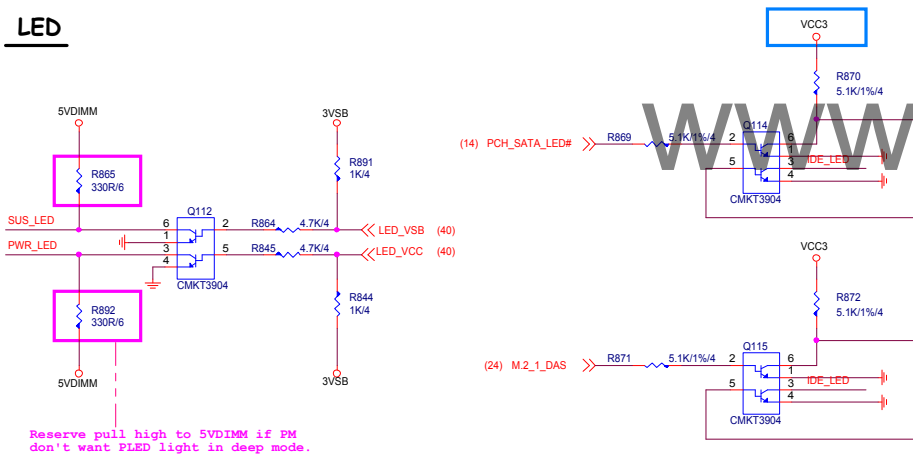
ATX POWER CONNECTOR



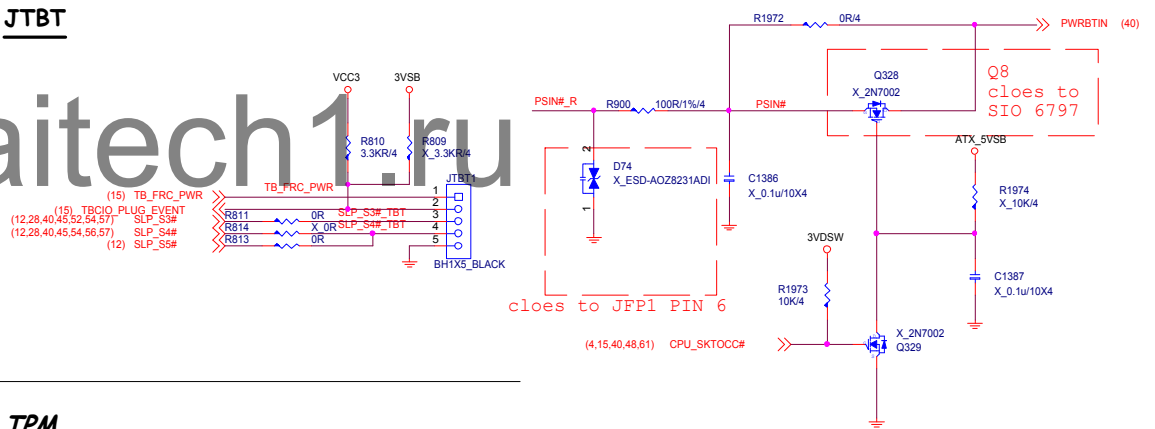
Front Panel



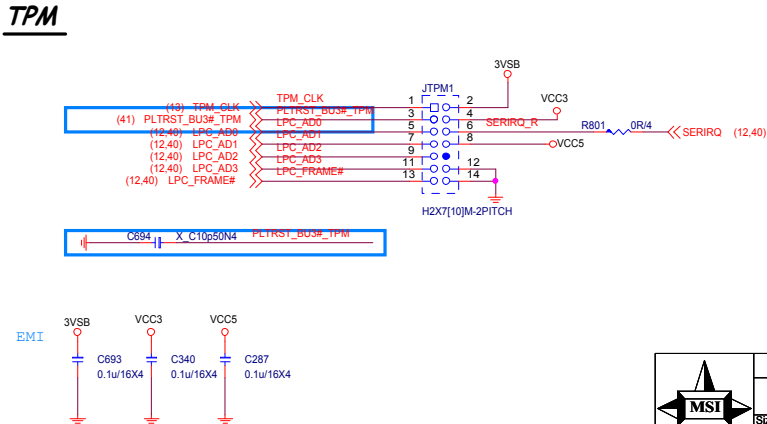
LED



JTBT



TPM



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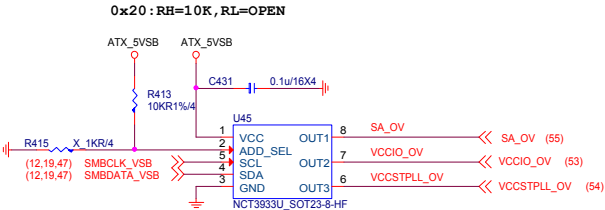
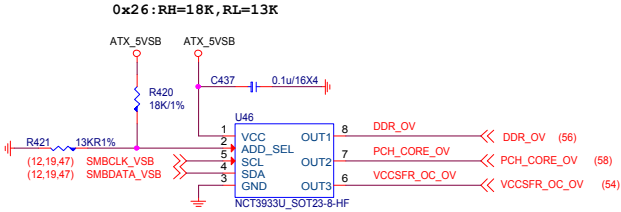
MS-7B49

Size Custom	Document Description ATX Power/F_Panel	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 46 of 69

Over Voltage Control IC

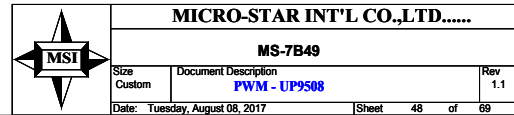
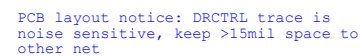
UPI VOLTAGE CONSOLE

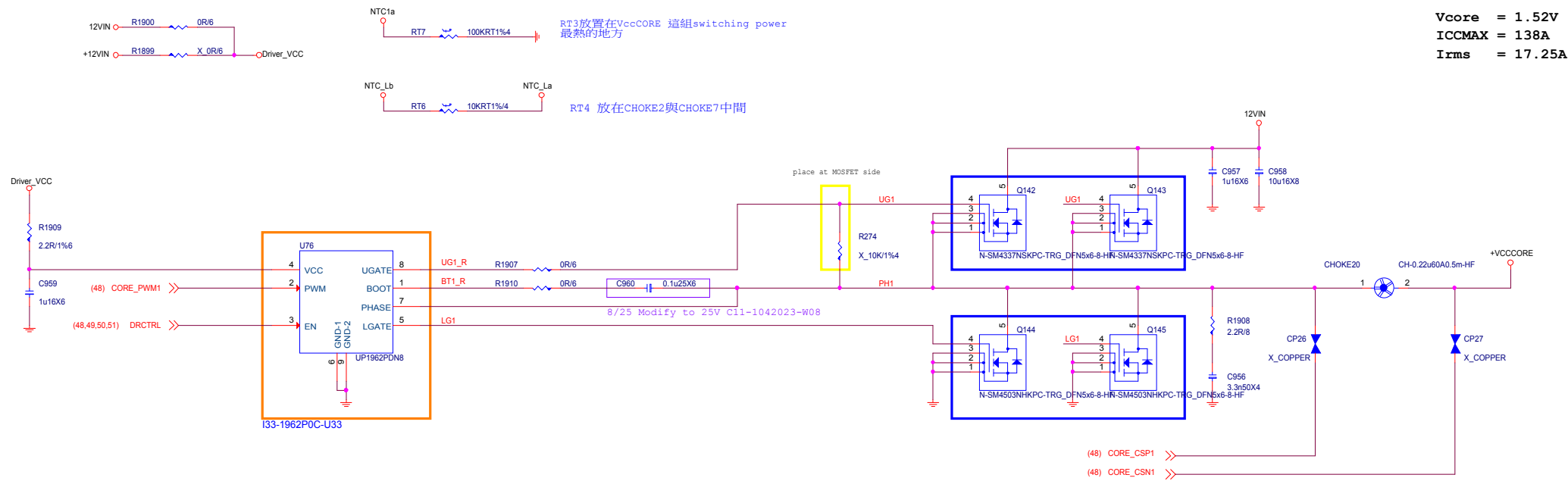
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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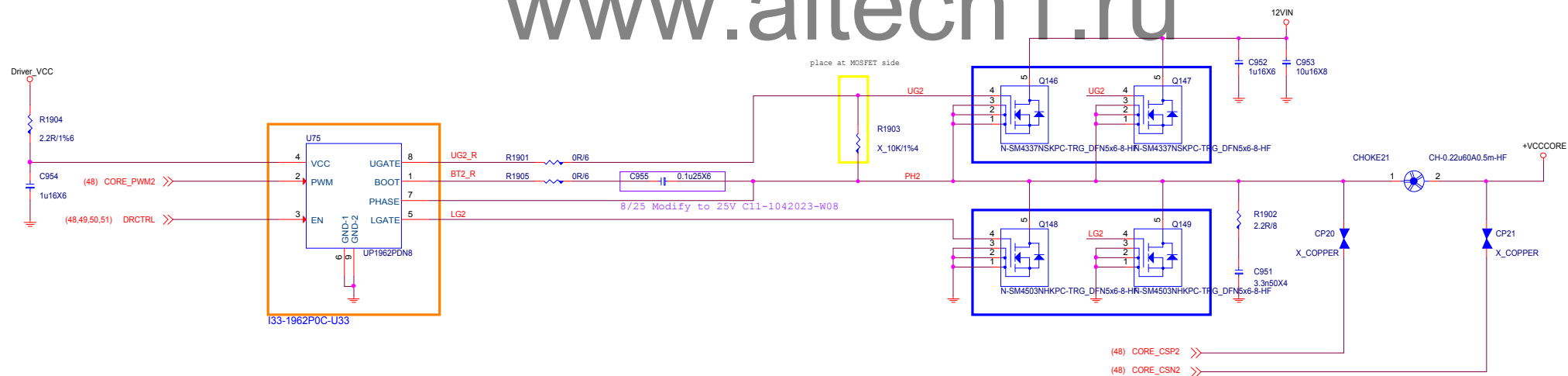
VGT: ICC Max 45A
LL: 3.1 mohm
OCP: 75A





Vcore = 1.52V
ICCMAX = 138A
Irms = 17.25A

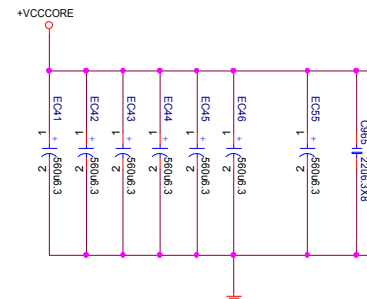
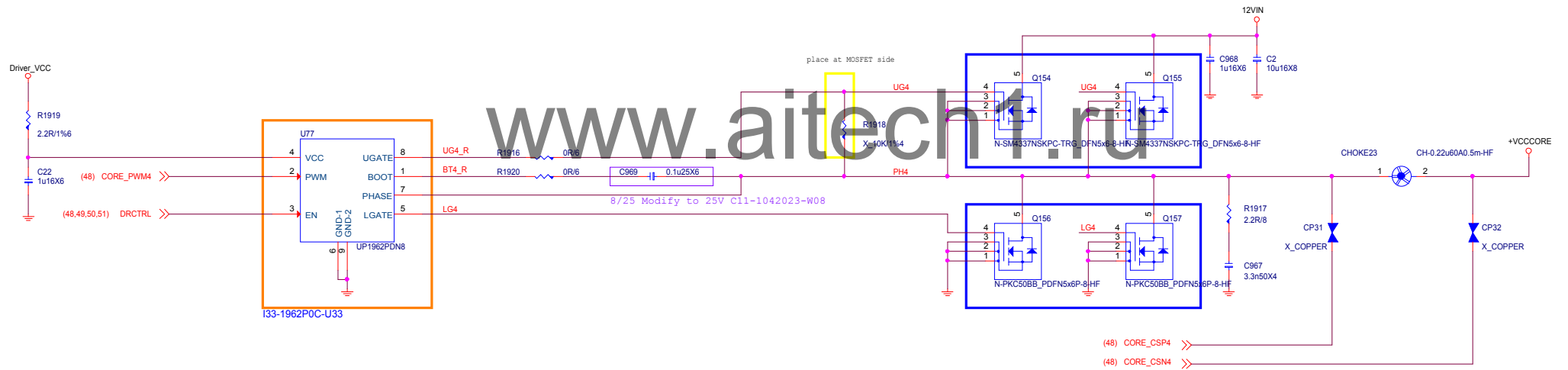
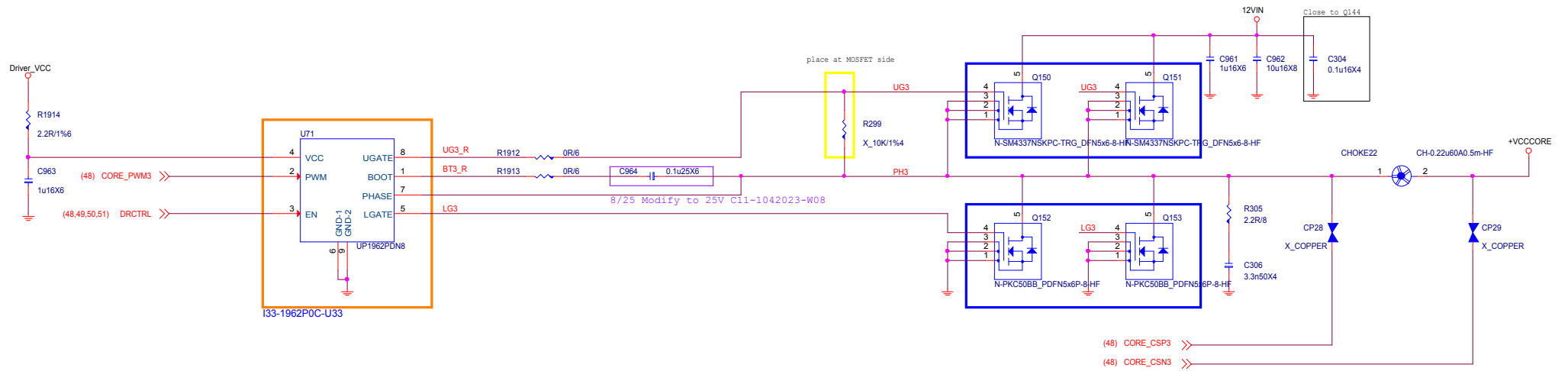
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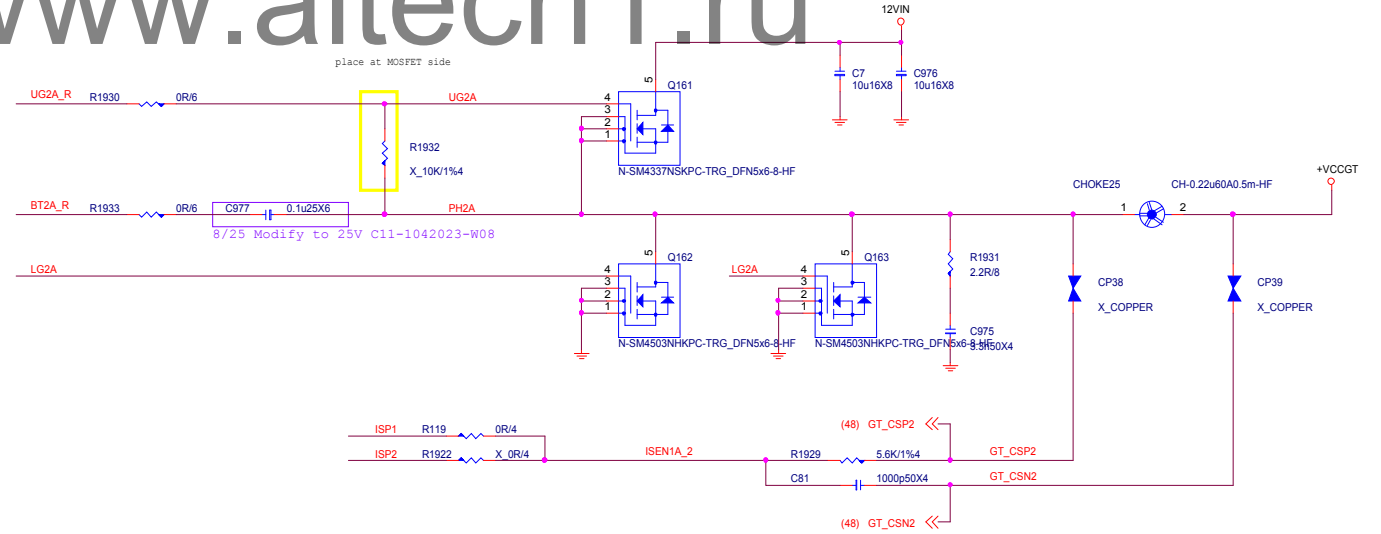
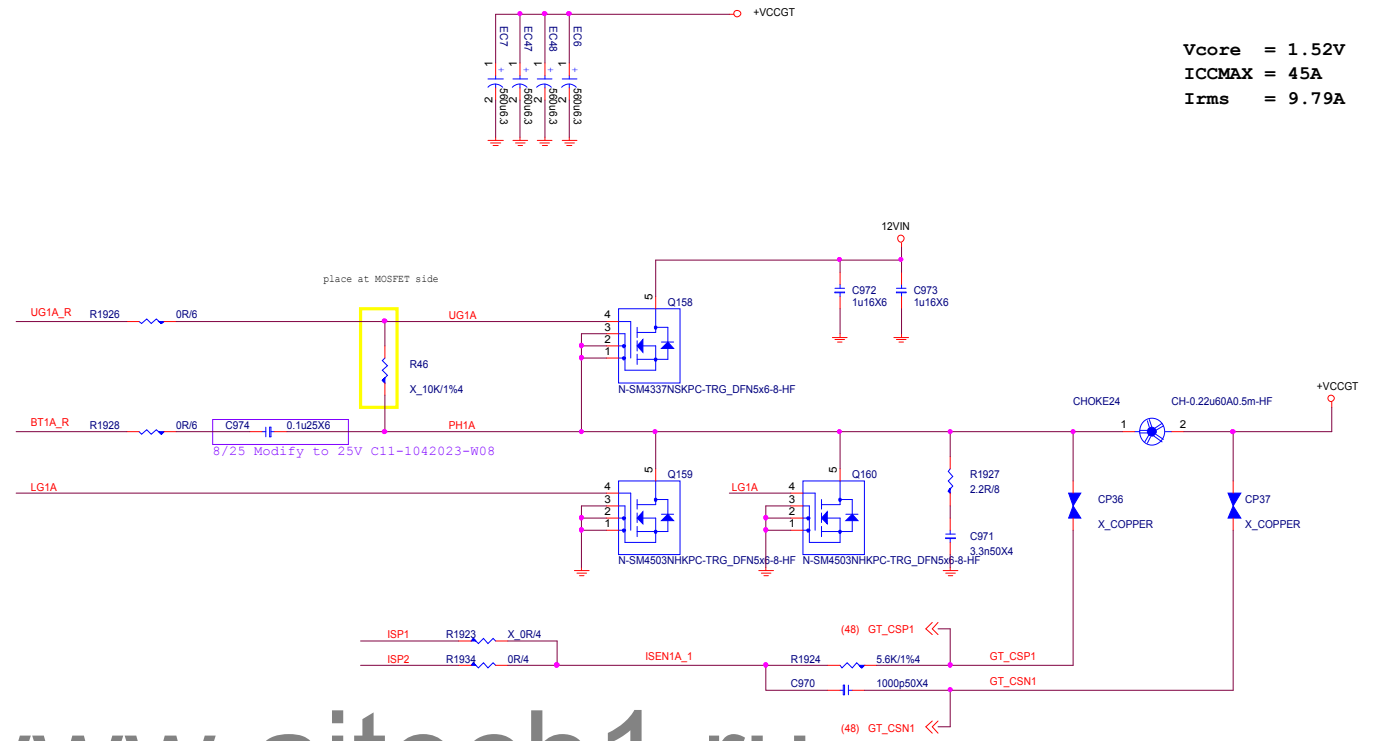
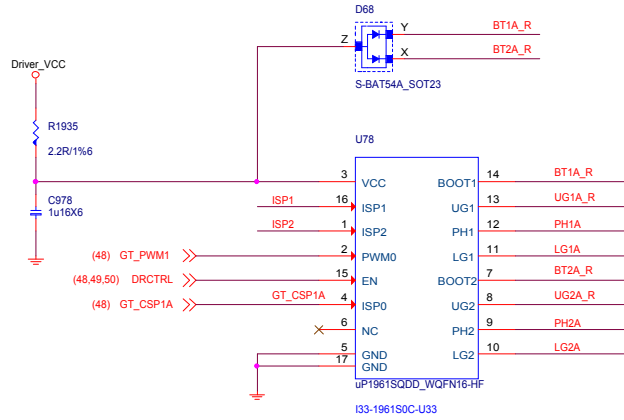
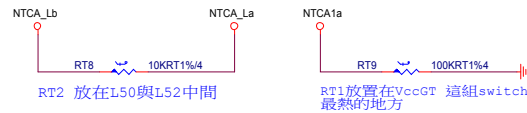
Size	Document Description	Rev
Custom	VCORE - PHASE 1-2	1.1
Date: Tuesday, August 08, 2017	Sheet 49 of 69	



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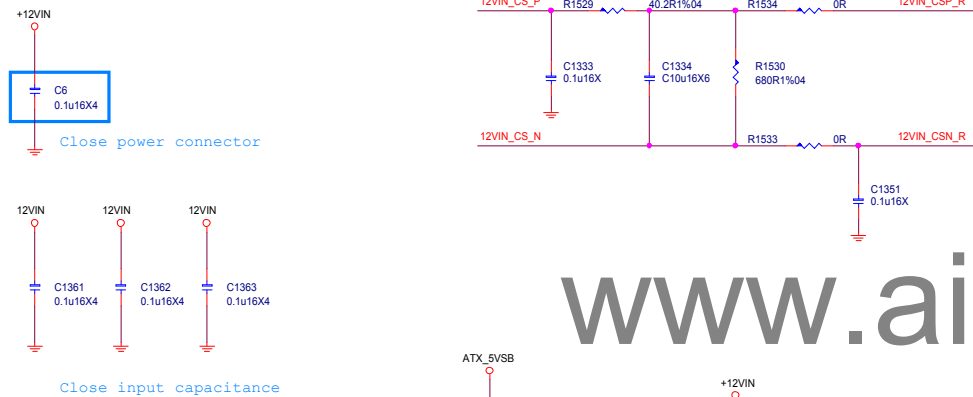
MS-7B49

Size	Document Description	Rev
Custom	VCORE - PHASE 2-4	1.1
Date: Tuesday, August 08, 2017	Sheet 50 of 69	

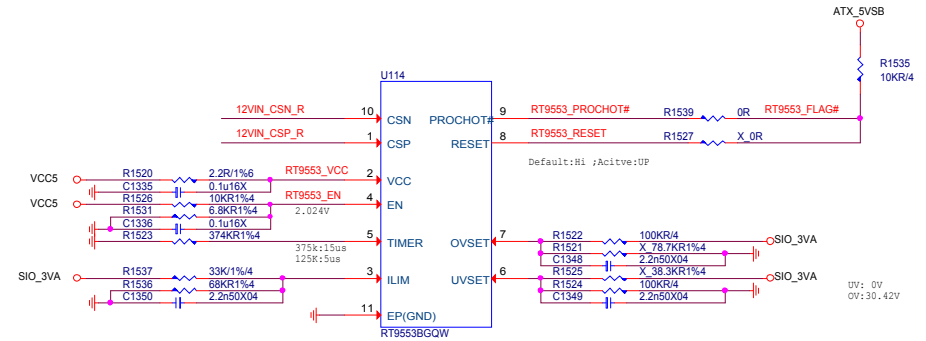


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```
Iripple = 27.04A
VCORE   = 17.25A
VGT      = 9.79A
```

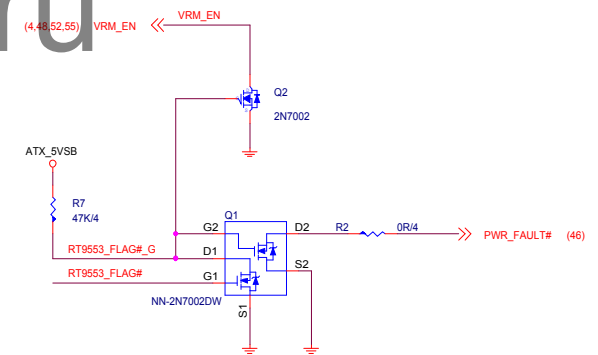


www.aitech1.ru (4,48/52,55)



R17+R18>100k Vsio_3va= 3.33V Rdcr= 0.58 mohm

```
I3933_imon*[R17*R18/(R17+R18)]= Istep* RdcR*100
I3933_imon= 10uA/step
Istep=4.785A
```

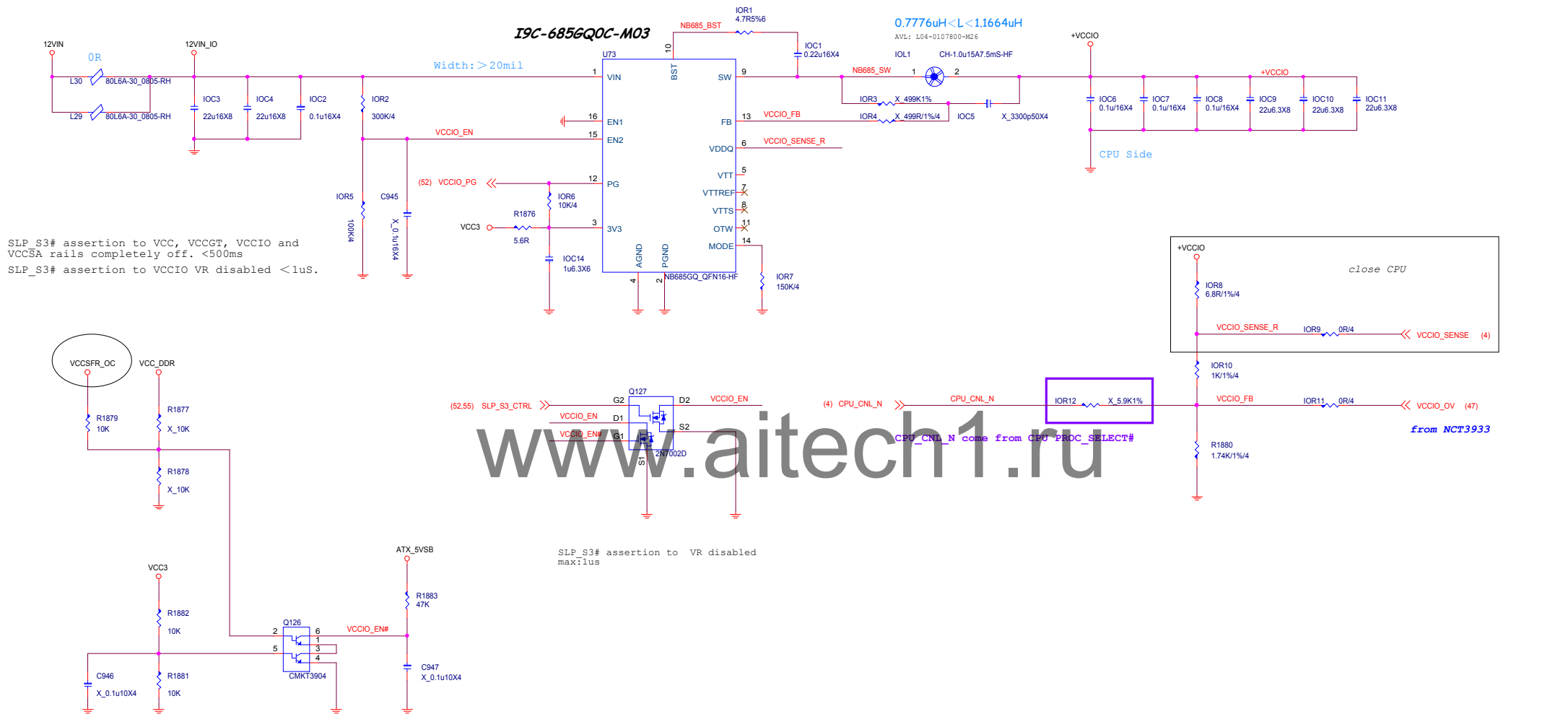


VCCIO

0.95V ; 6.4A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685



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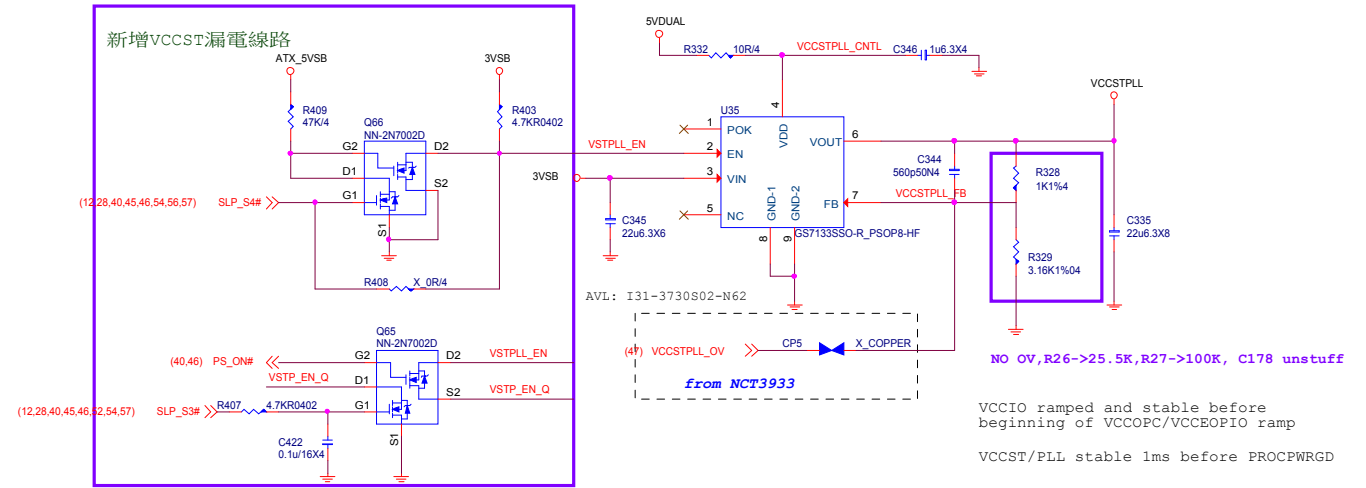
Size	Document Description	Rev
Custom	VCCIO - NB685	1.1
Date: Tuesday, August 08, 2017	Sheet 53 of 69	

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

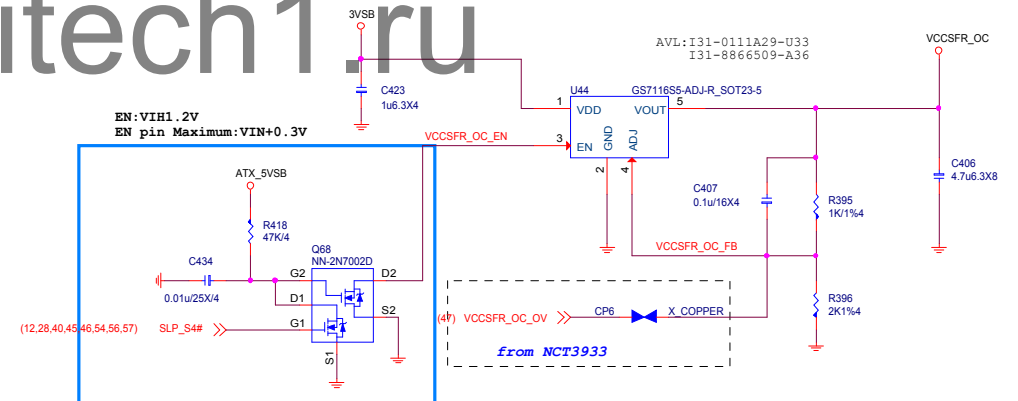
for Gaming3/5, Classic, ECO and H110



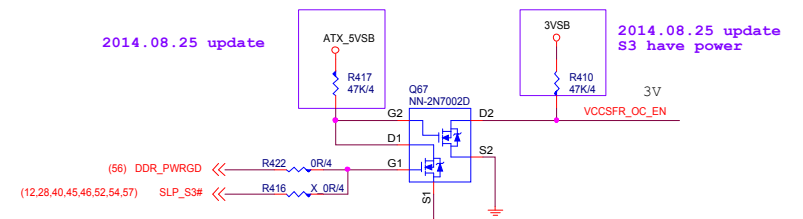
VCCPLL_OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



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MS-7B49			
Size	Document Description	Rev	
Custom	VCCST/PLL - GS7133/7116	1.1	
Date:	Tuesday, August 08, 2017	Sheet	54 of 69

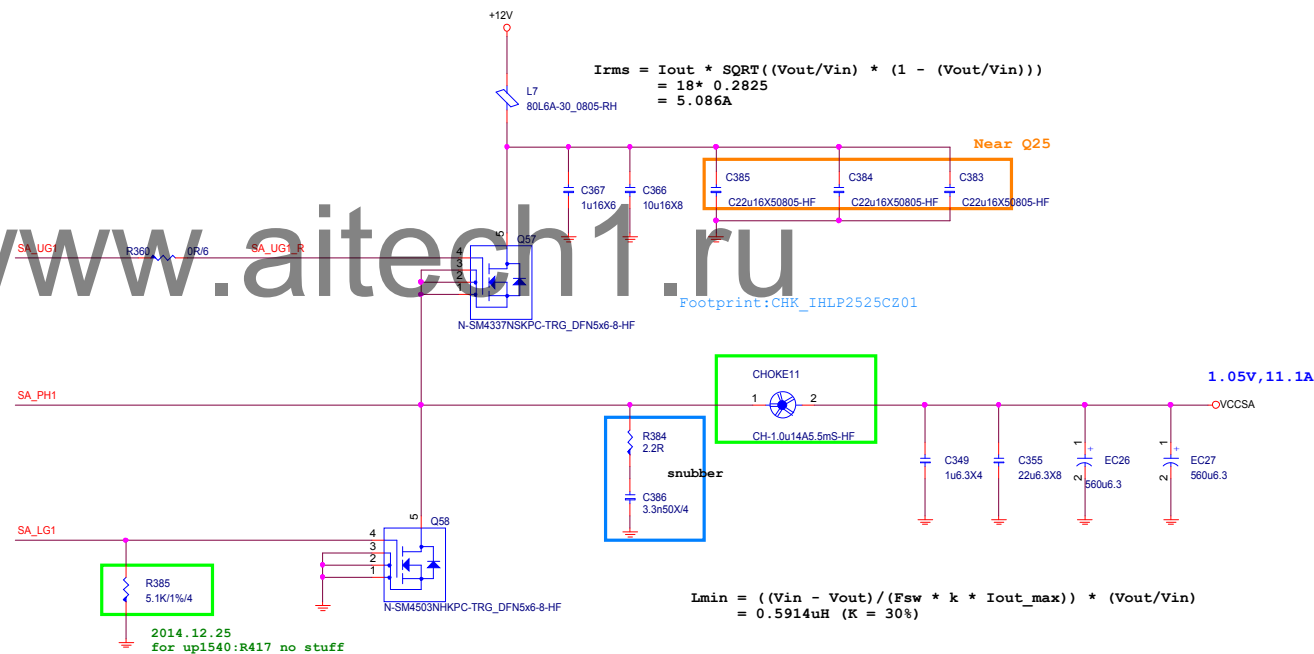
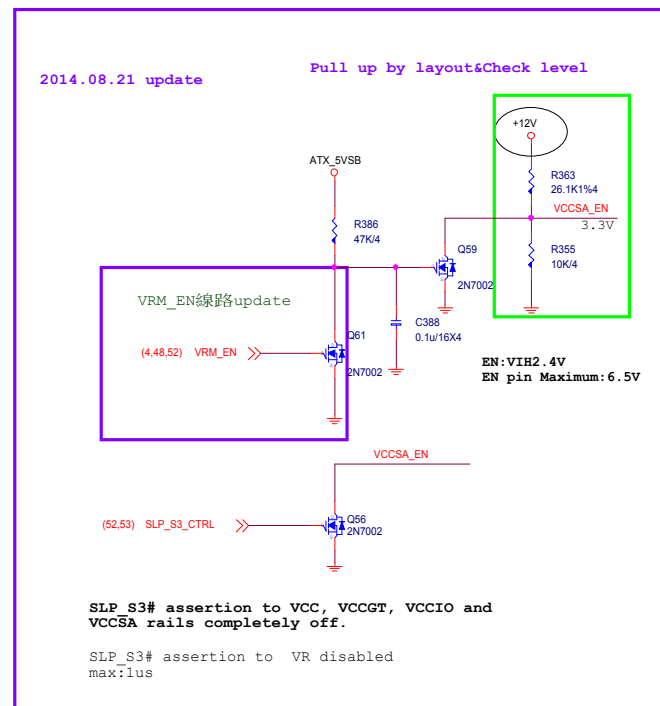
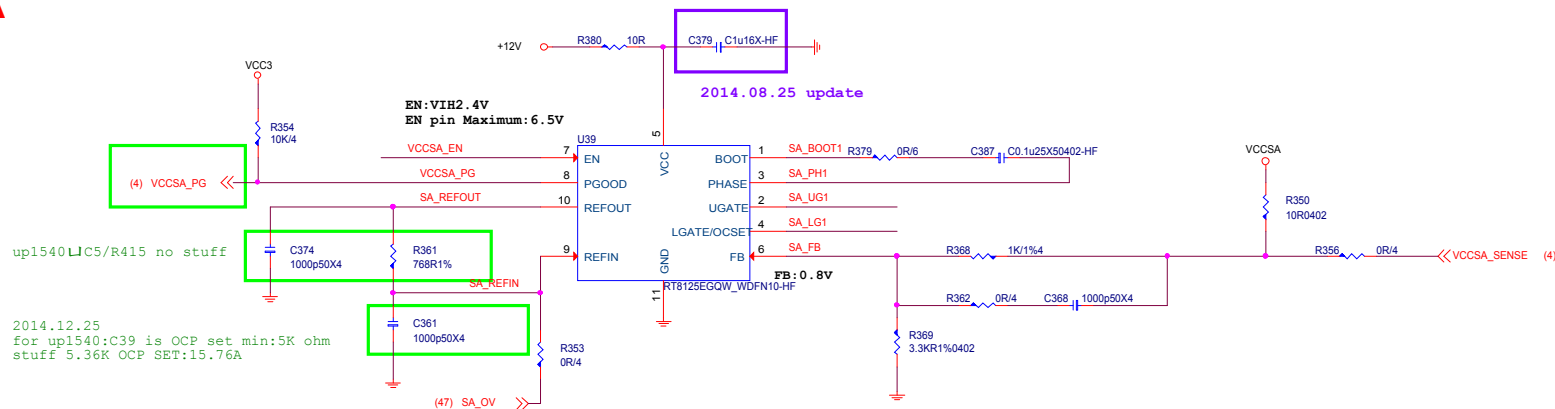
SA Power:1.05V,11.1A

Rocpset:5.6K
OCP=Rocset*Rdson(Low side)/10uA
=5.1K*3mohm/10uA
=19A

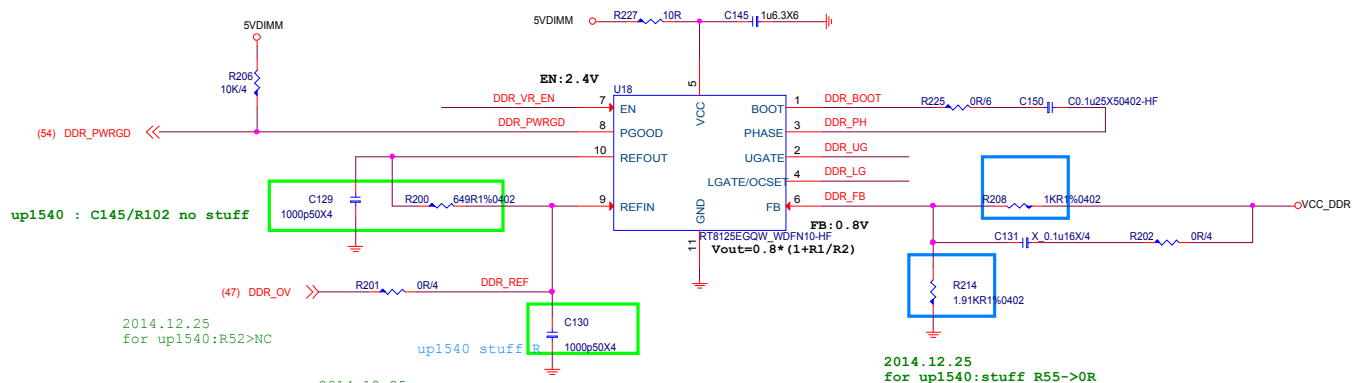
Rocs:5.76K,OCP:
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm
use UBIQ MOS need Check

Rdson(Low) 10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

Vsa = 1.05V
ICCMAX = 11.1A
Irms = 3.14A



3.3A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

$$\begin{aligned} \text{Rocpset} &= 4.32\text{K} \\ \text{OCP} &= \text{Rocpset} * \text{Rdson}(\text{Low side}) / 10\mu\text{A} \\ &= 8.2\text{K} * 10\mu\text{A} / 4\text{mohm} \\ &= 20.5\text{A} \end{aligned}$$


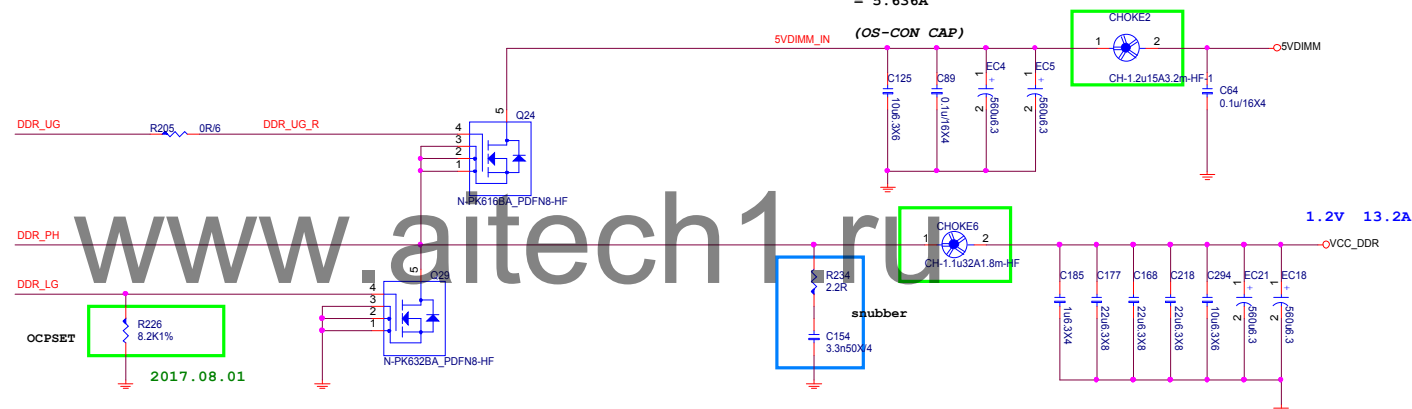
Rdson (low) 4.5V

D03-4C05N03-O05	:	5 mohm
D03-632BA0C-N03	:	4.6mohm
D03-3056M00-U47	:	6.2mohm

```
2014.12.25
for up1540:R52>NC
```

up1540 stuff R 1000p50X4

C125 is OCP set min:5K ohm
5.1K OCP SET:22.173A

$$\begin{aligned} I_{rms} &= I_{out} * \text{SQRT}\{(V_{out}/V_{in}) * [1 - (V_{out}/V_{in})]\} \\ &= 13.2 * 0.427 \\ &= 5.636A \end{aligned}$$


Datasheet公式計算

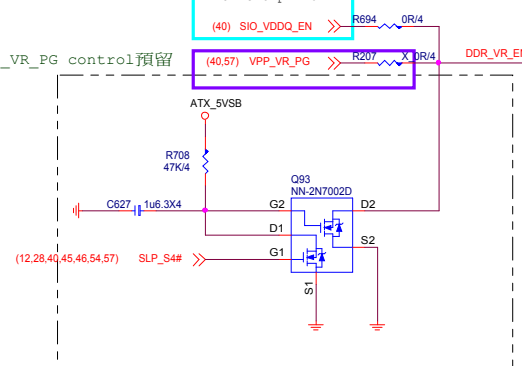
$$\begin{aligned} L_{\min} &= ((V_{\text{in}} - 1.2V) / (F_{\text{sw}} * k * I_{\text{out_max}})) * (V_{\text{out}} / V_{\text{in}}) \\ &= 0.7677\mu\text{H} \quad (K = 30\%) \end{aligned}$$

若帶入CAP ESR計算, $0.2432\mu\text{H} < L < 1.2897\mu\text{H}$

2014.12.17 update

From SIO pin 87

VPP_VR_PG control預留

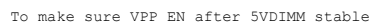


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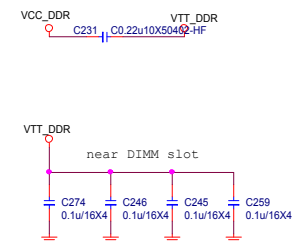
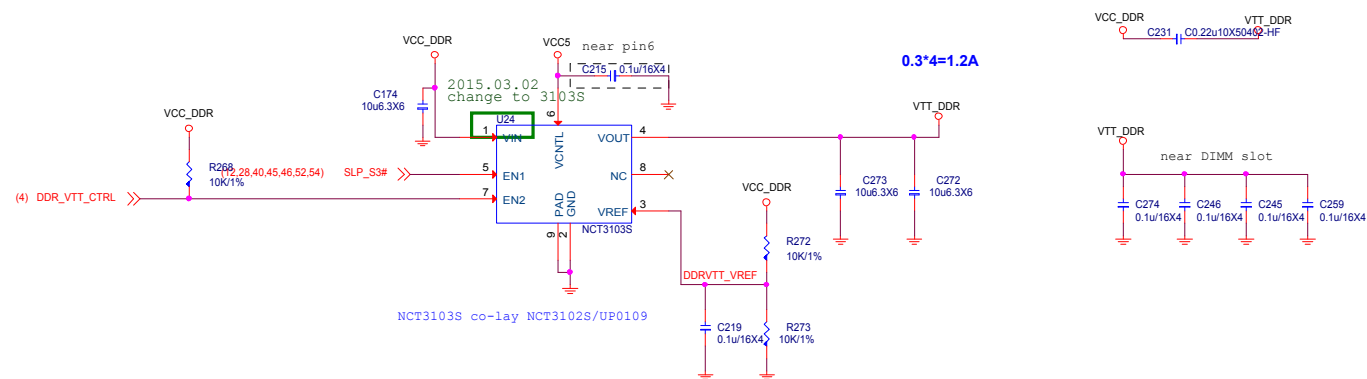
MS-7B49

Size Custom	Document Description DDR4 Power-RT8125C	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 56 of 69

VPP25 Power
2.5V; 2.24A



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$$0.3 \times 4 = 1.2A$$


MS-7B49

Size Custom	Document Description DDR4 Power-VPP25	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 57 of 69

PCH 1VSB

1.0V; 11A

Rocpset: 6.8K
 OCP=Rocset*10uA/Rdson(Low side)
 =6.8K*10uA/4mohm
 =17A

Rocs: 7.87K, OCP:
 D03-4C05N03-O05 : 15.74A
 D03-632BA0C-N03 : 17.1A
 use UBIQ MOS need Check

Rdson(Low) 4.5V

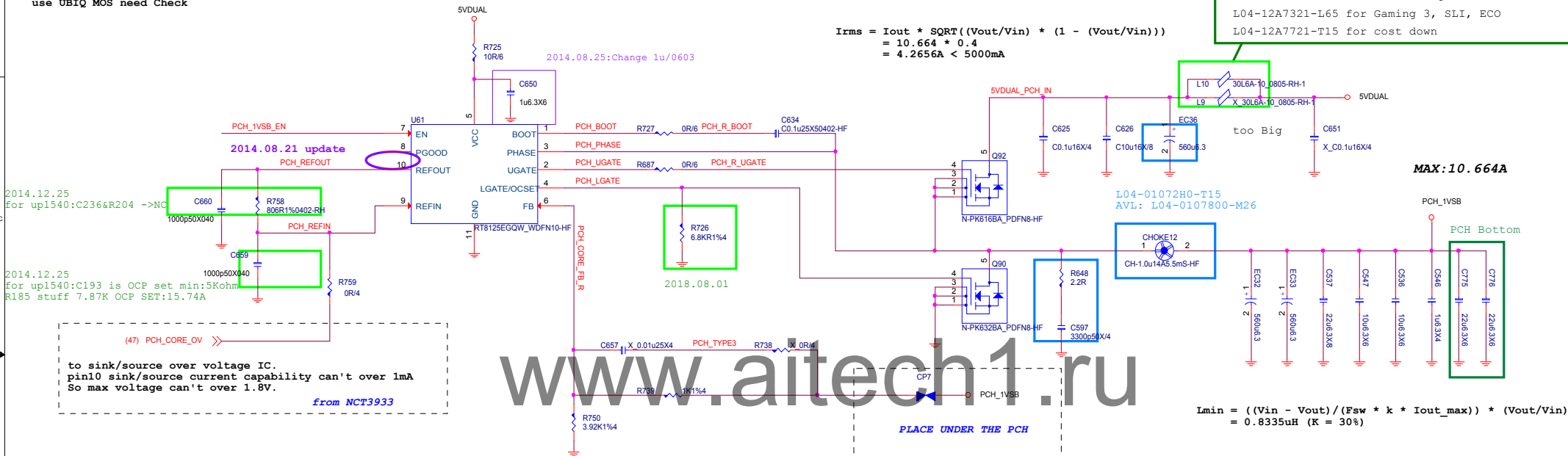
D03-3116M00-U47 : 3.6 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
 L04-12A7321-L65 for Gaming 3, SLI, ECO
 L04-12A7721-T15 for cost down



MAX: 10.664A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

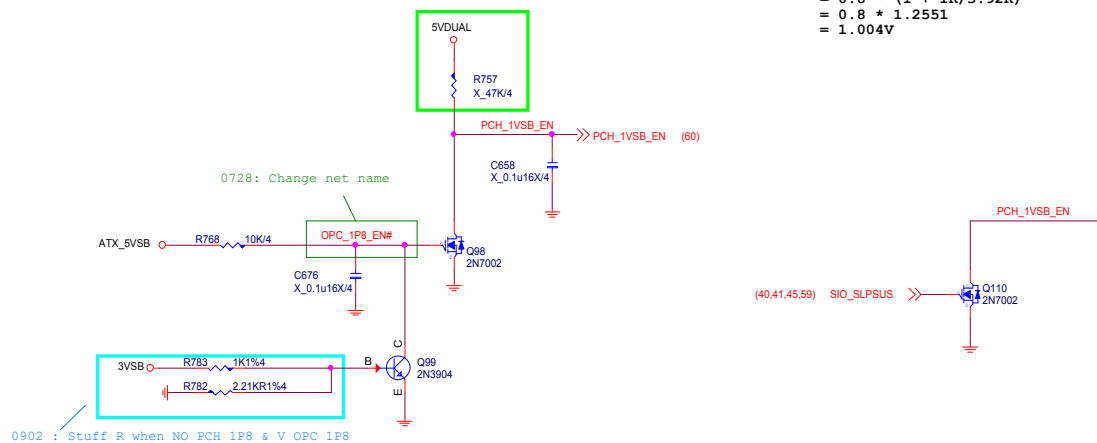
$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

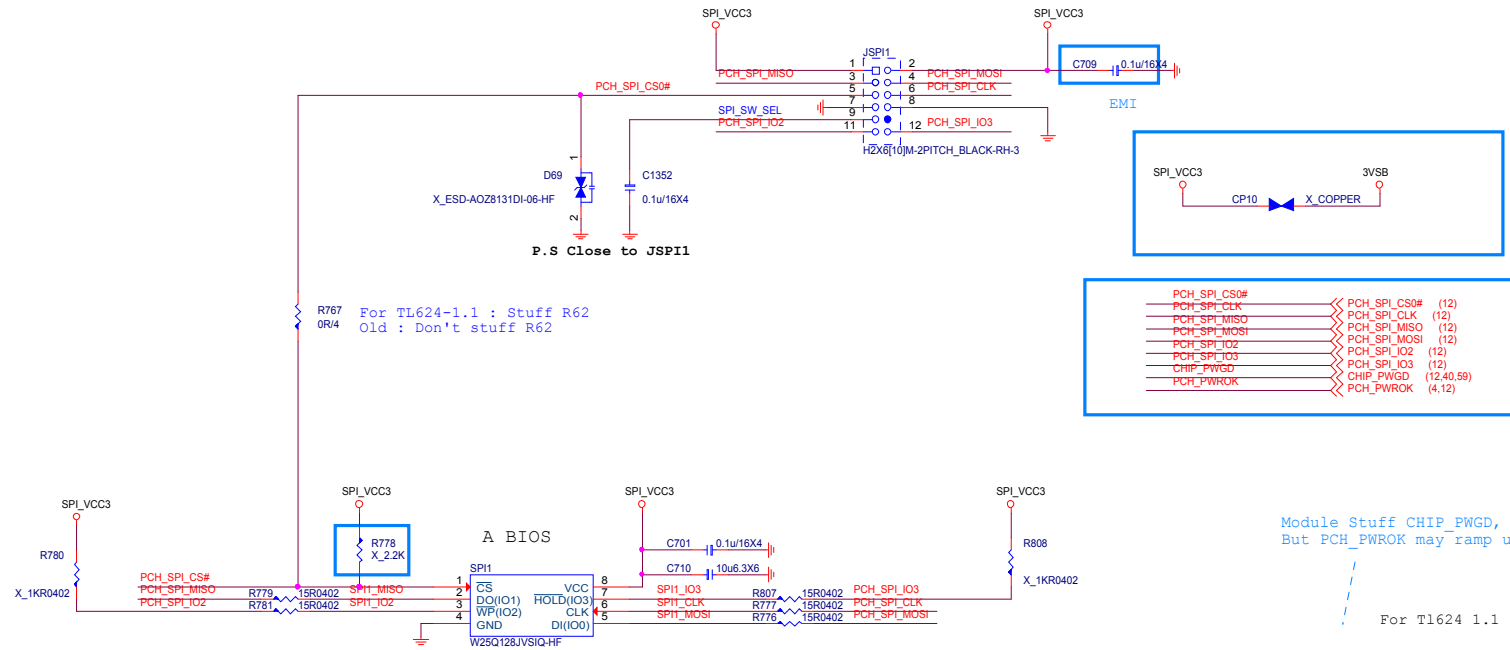
$$= 1.004V$$



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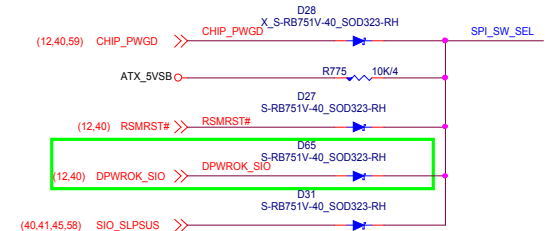
Size	Document Description	Rev
Custom	PCH Power - RT812SE	1.1
Date: Tuesday, August 08, 2017	Sheet 58 of 69	



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Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

For TL624 1.1



For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272



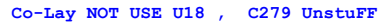
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MS-7B49

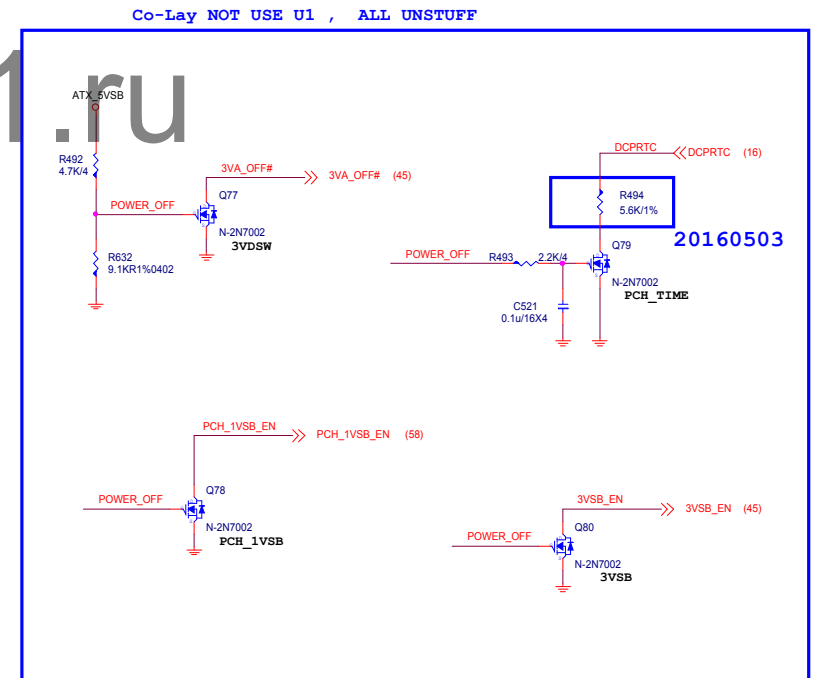
Size	Document Description	Rev
Custom	SPI ROM	1.1
Date: Tuesday, August 08, 2017	Sheet 59 of 69	

Default

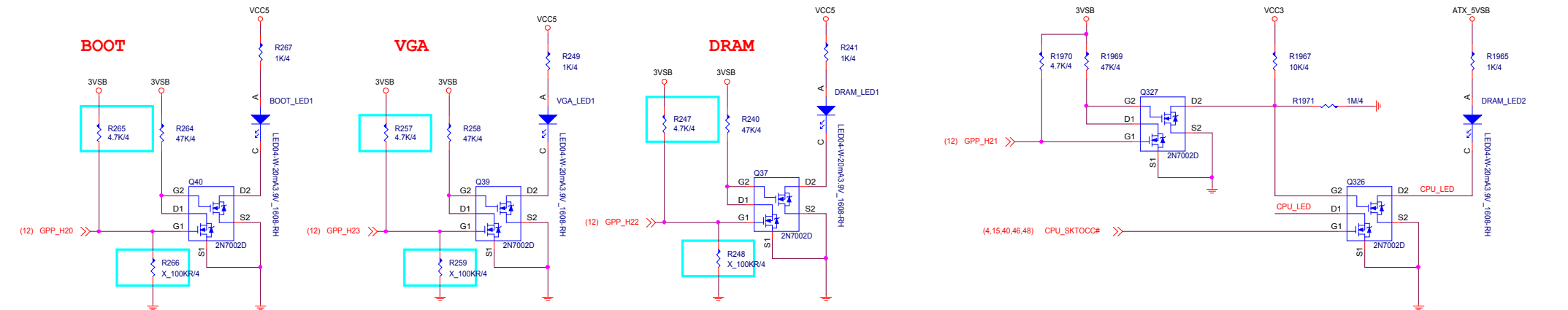
Default



If has discharge function R15 change to ESD.
ESD"D0G-2950500-SI0"

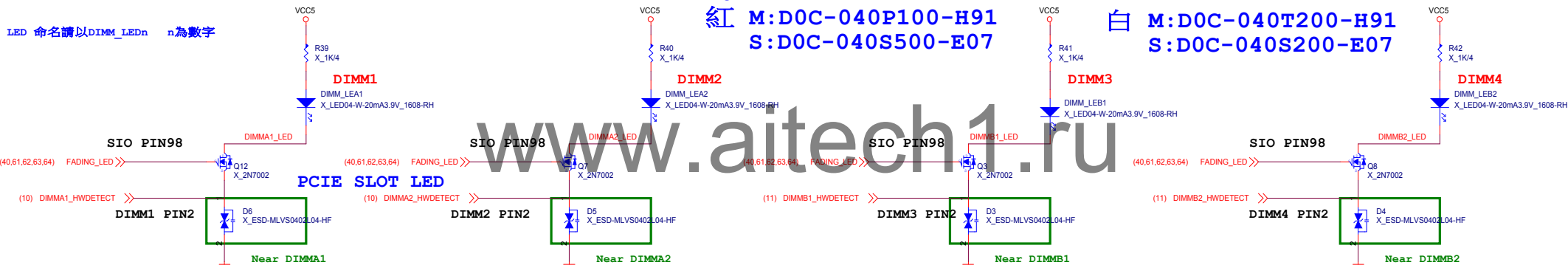


EZ Debug



DIMM

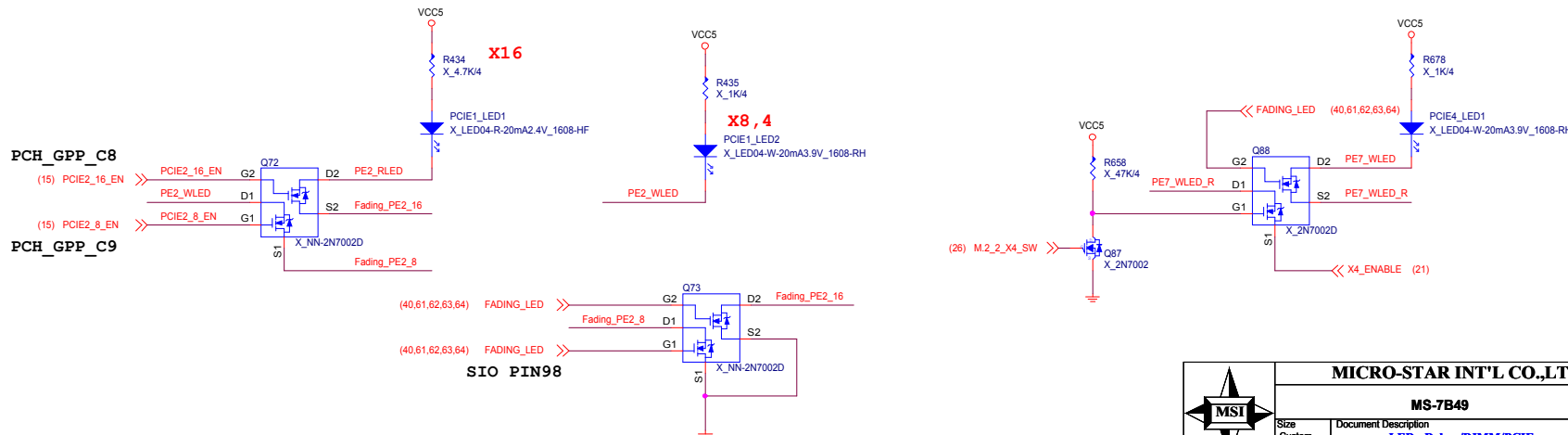
LED 命名請以DIMM_LEDn n為數字



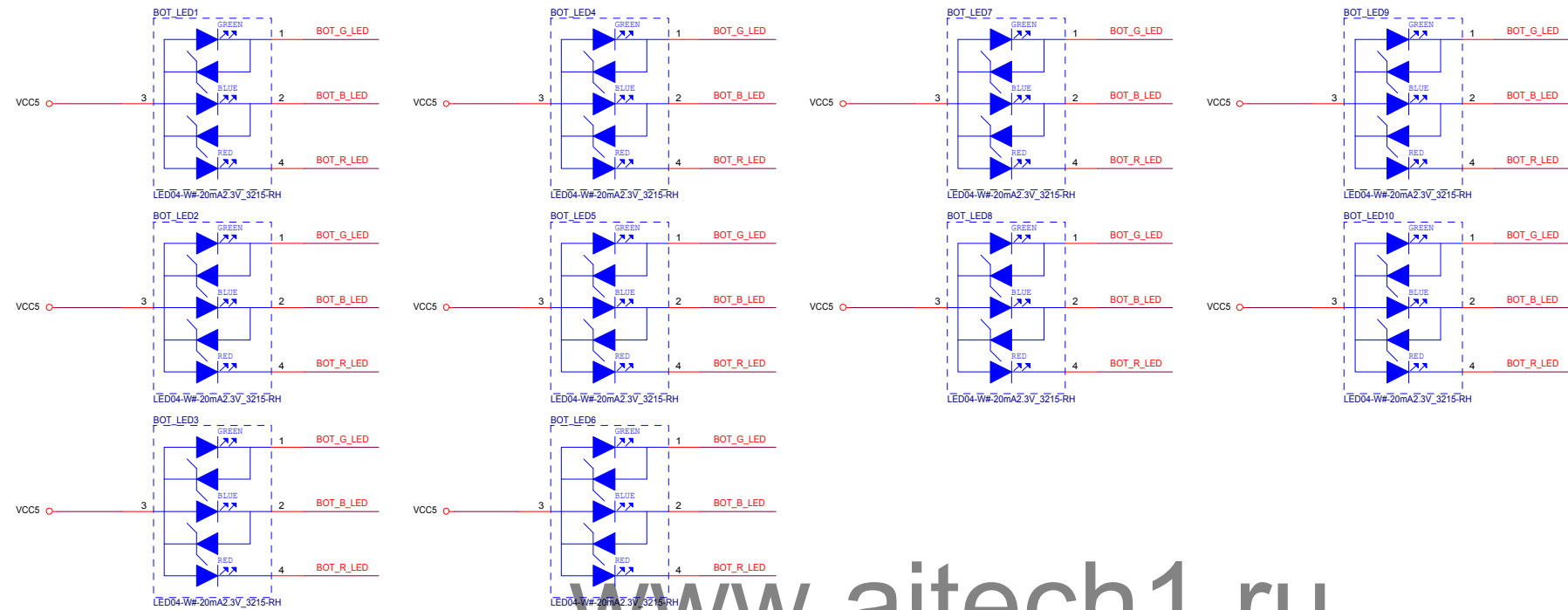
PCIE

PCIE SLOT LED 命名請以PCIE_LEDn n為數字

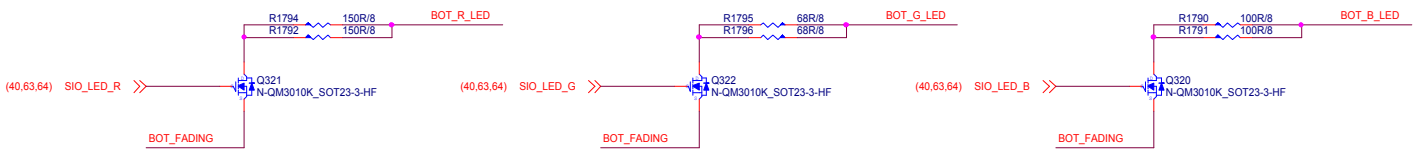
GPIO LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)



BOTTOM LED



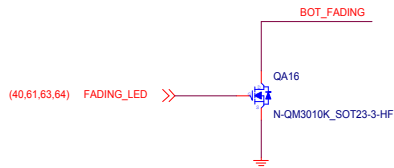
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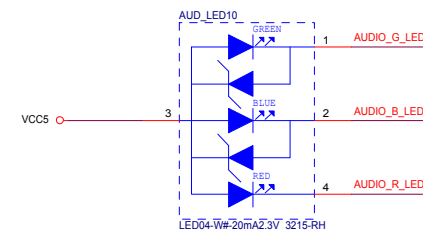
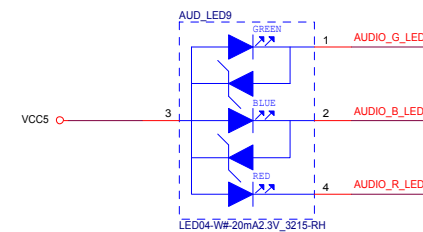
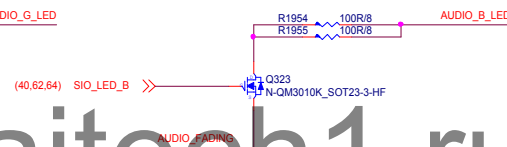
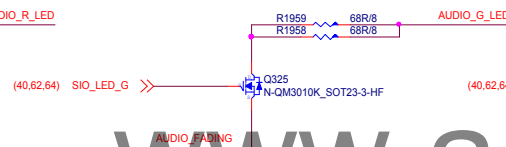
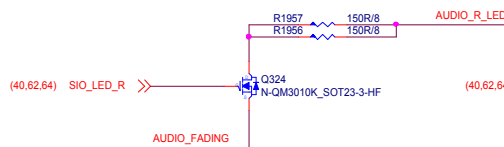
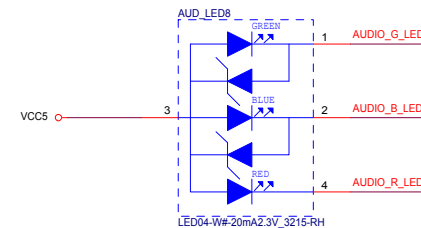
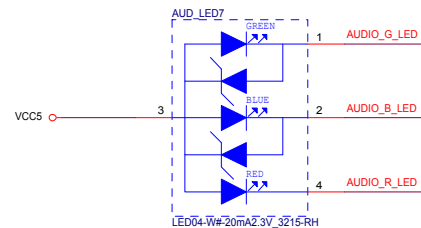
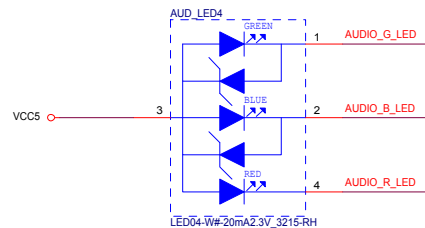
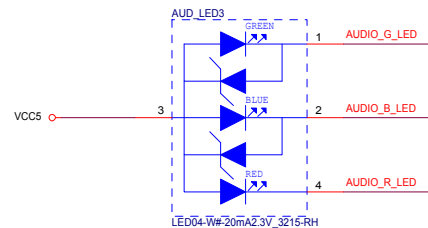
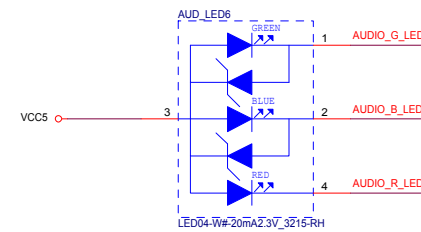
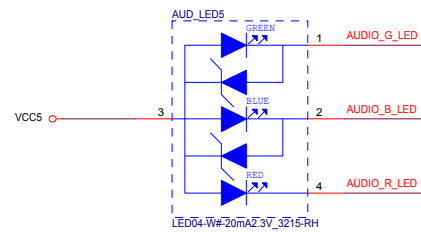
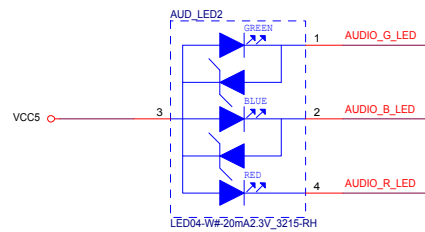
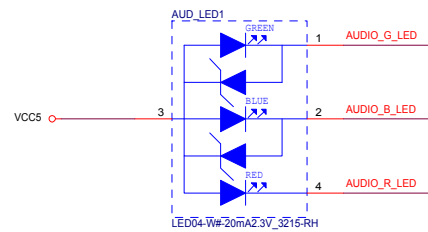
Vf=1.7 V~2.3V
5.05V-1.9V/27.3=0.115A
0.115A*0.115A*27.3=0.36W
PS:實際量測LED Vf=1.9v

Vf=2.7 V~3.45V
5.05V-2.8V/27.3=0.0824A
0.0824A*0.0824A*27.3=0.185W
PS:實際量測LED Vf=2.8v

Vf=2.7 V~3.45V
5.05V-2.9V/27.3=0.0787A
0.0787A*0.0787A*27.3=0.169W
PS:實際量測LED Vf=2.9v



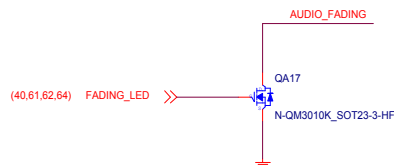
AUDIO LED



Vf=1.7 V~2.3V
 $5.05V - 1.9V / 27.3 = 0.115A$
 $0.115A * 0.115A * 27.3 = 0.36W$
 PS: 實際量測LED Vf=1.9v

Vf=2.7 V~3.45V
 $5.05V - 2.8V / 27.3 = 0.0824A$
 $0.0824A * 0.0824A * 27.3 = 0.185W$
 PS: 實際量測LED Vf=2.8v

Vf=2.7 V~3.45V
 $5.05V - 2.9V / 27.3 = 0.0787A$
 $0.0787A * 0.0787A * 27.3 = 0.169W$
 PS: 實際量測LED Vf=2.9v



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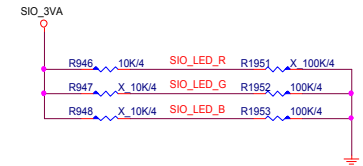
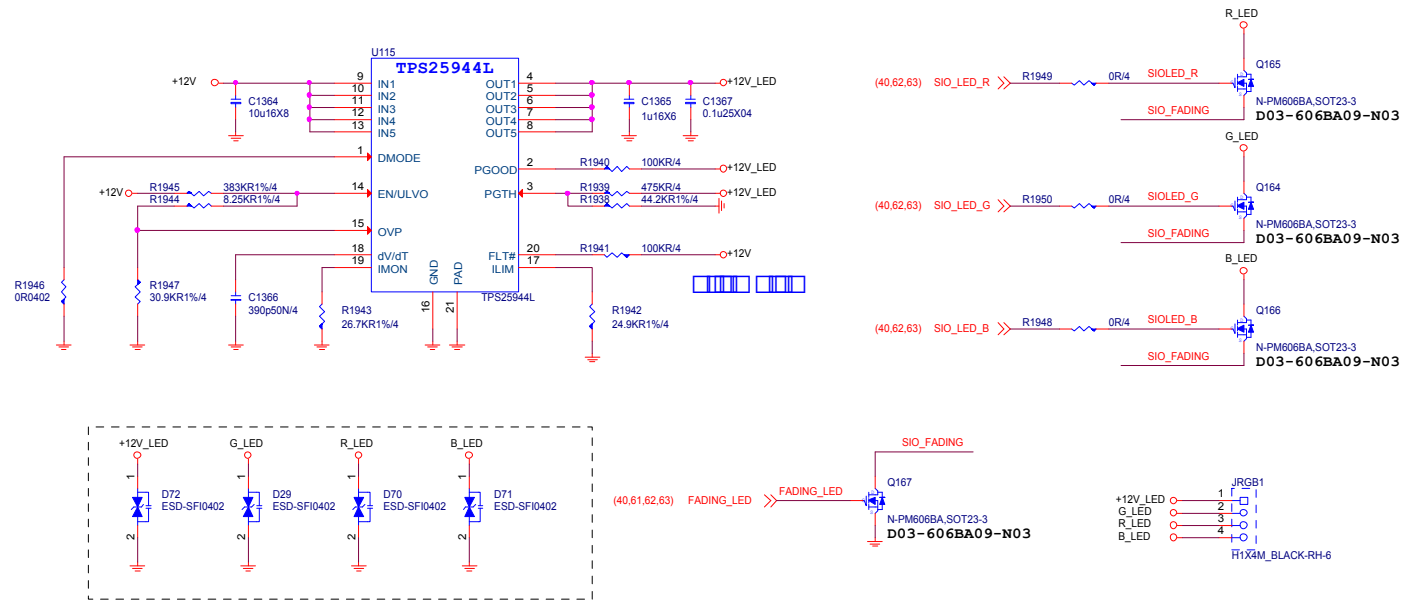


MICRO-STAR INT'L CO.,LTD

MS-7B49

Size	Document Description	Rev
Custom	LED - Debug/DIMM/PCIE	1.1
Date: Tuesday, August 08, 2017	Sheet 63 of 69	

LED Control by SIO



Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

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MICRO-STAR INT'L CO.,LTD

MS-7B49

Size Custom	Document Description LED - Debug/DIMM/PCIE	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 64 of 69

CPU Socket



Battery



BIOS Label

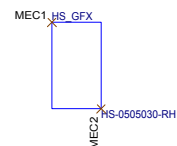


PCB

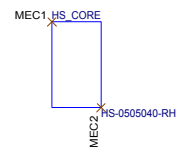


PD0-07B4911-G37, 精成-深圳, 1, 台北微星廠 (MSI)
PD0-07B4911-E48, 競華, 1, 台北微星廠 (MSI)

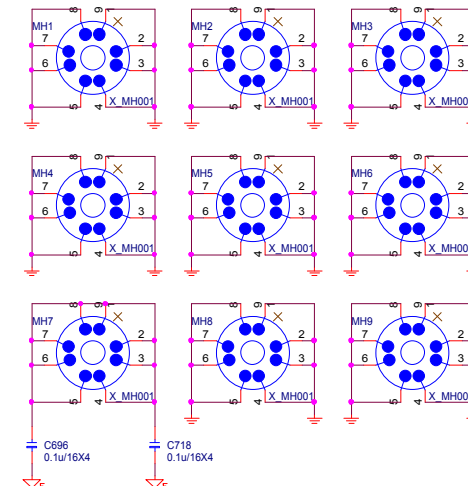
GFX Heatsink



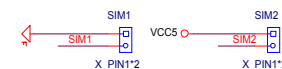
CORE Heatsink



Mounting Holes



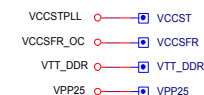
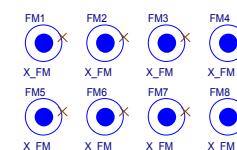
Simulation



Test point



Optical Fiducial Marks-120



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MS-7B49

Size	Document Description	Rev
Custom	Manual parts	1.1
Date: Wednesday, August 09, 2017	Sheet 65 of 69	

To POWER 2015/02/03